High voltage IGBT/Diode module Application Manual

Minebea Power Semiconductor Device Incorporated

October/2025

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This is a safety warning symbol. It is used to alert you to potential hazards that could cause harm to people. To avoid possible injury or death, follow the safety messages that accompany this symbol.

Danger : Indicates a hazardous situation which, if not avoided, will result in death or serious injury.

Warning : Indicates a hazardous situation which, if not avoided, could result in death or serious injury.

Caution : Indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.

Notice : Indicates information considered important, but not hazard-related (e.g., messages relating to property damage).

※*Serious injuries mentioned above refer to those that result in lasting effects such as blindness, injuries, burns (high or low temperature), electric shock injuries, fractures, poisoning, and those requiring hospitalization or long-term outpatient care for treatment. Moderate or minor injuries refer to injuries, burns, electric shock injuries, etc., that do not require hospitalization or long-term outpatient care for treatment. Non-personal injuries refer to damages unrelated to personal injury, such as property damage, product malfunction or breakage, data loss, and other non-personal injury-related damages.*

Safety Precautions

＜ Common Safety Precautions ＞

- When designing electronic circuits, please ensure that the device is used within the specified "absolute maximum ratings" under any external condition changes (within the guaranteed range). Additionally, for pulse applications, ensure that the ratings do not exceed the "safe operating area (SOA).“

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- Perform actual load tests that cover the conditions of current, voltage, frequency, pulse width, etc., that may occur in actual high-current load tests.

- IGBT modules integrated into power conversion systems, such as inverters, undergo repeated temperature fluctuations due to self-heating caused by power dissipation. These temperature variations subject the IGBT modules to thermal stress. Ensure that the modules are operated under conditions where the IGBT module lifetime limited by thermal stress is equal to or longer than the designed service life of the equipment. For further details, please refer to Section 3-7-5, "Power cycle lifetime in actual devices".

The following warning labels are related to semiconductor devices. Failure to comply with these warning labels may result in a risk of death or serious injury. Please note that the order of this list does not indicate the order of importance. Each item is equally important.

⚠ **Warning**	Page
(7-1-1. Warning about package rupture) ●If a load short-circuit or arm short-circuit occurs, turn off the IGBT module within a short period (approximately a few microseconds). The package may burst.	7-1
(7-1-2. Warnings for Burns and Electric Shock) ●While the power is on, do not touch or approach the product. There is a risk of burns and electric shock.	7-1

The following caution labels are related to semiconductor devices. Failure to comply with these caution labels may result in minor injury or material damage only. Please note that the order of this list does not indicate the order of importance. Each item is equally important.

⚠ Caution	Page
(Chapter 2. Specification Details) ●When designing electronic circuits using semiconductor devices, ensure that the specified 'absolute maximum ratings' of the device are not exceeded under any external condition changes. Additionally, for pulse applications, ensure that the ratings of the 'safe operating area (RBSOA/RRSOA)' are not exceeded.	2-1
(7-2. Cautionary Notes) ●After IGBT failure, ensure that short-circuit current does not flow for an extended period (approximately several hundred microseconds). There is a risk of smoke and fire.	7-1

Caution

1. Please note that the contents of this document are subject to change without notice.

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＜About RoHS＞

The RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive is a regulation on hazardous substances enforced by the EU (European Union) on July 1, 2006, which prohibits the inclusion of specific hazardous substances in electrical and electronic equipment.

Currently, the regulated substances are lead (Pb), cadmium (Cd), hexavalent chromium (Cr^{6+}), mercury (Hg), polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE), bis(2-ethylhexyl) phthalate (DEHP), benzyl butyl phthalate (BBP), dibutyl phthalate (DBP), and diisobutyl phthalate (DIBP).

Regarding the regulatory concentration (threshold), cadmium is limited to 0.01wt% (100ppm), while all other prohibited substances are limited to 0.1wt% (1000ppm). Products containing these 10 substances above the threshold (0.01% for Cd, 0.1% for others) cannot be sold within the EU. However, exemptions are granted for applications where technical substitution is difficult.

In relation to RoHS compliance for IGBT and Diode modules, lead (Pb) contained in the solder used to connect each chip and DCB is particularly relevant. For information on the RoHS compliance status of our high-voltage IGBT and Diode modules, please refer to the status list published on our website.

Revision History

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Rev.1	3-1 Derating 3-7 Thermal Resistance and Heat Dissipation Design	2002.10.23	Katou	Saito	Koga
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Preface

This instruction manual provides specifications, main characteristics, various design guidelines (gate circuits, heat dissipation, protection circuits), and precautions for the use of high-voltage IGBT and Diode modules.

The contents of this instruction manual are subject to change without notice due to revisions and updates. For the latest information (detailed specifications and applications for each product), please refer to our website (https://www.minebea-psd.com).
If you have any questions, please contact our sales office listed below.

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Explanation of Terms and Abbreviations
For the terms and abbreviations used in this instruction manual, please refer to the table below.

Terms/abbreviations	Original word
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
FWD	Freewheeling Diode

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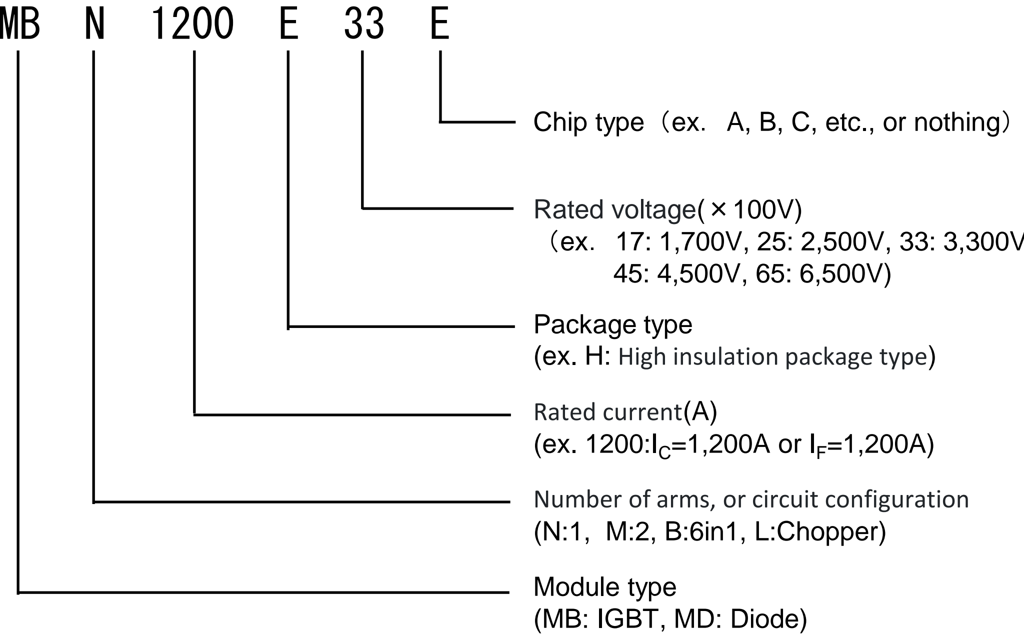
1. IGBT module

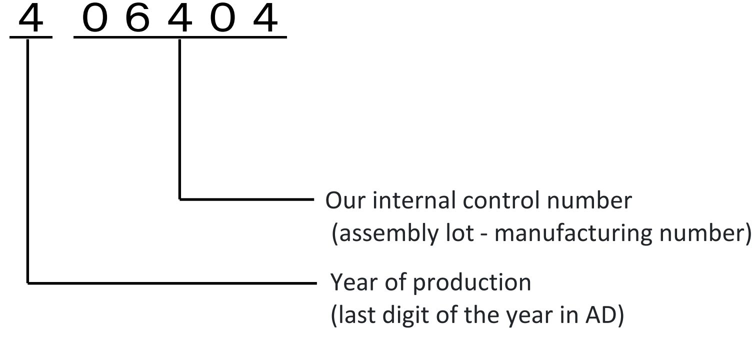
1-1. Type designation



1-2. Manufacturing lot number

In addition to the above format, the nameplate displayed on the product will also show the following manufacturing number.

Example of a manufacturing lot number ：



1-3. Basic Structure of the Module

Figure 1.1 shows a schematic cross-section of the internal structure of the IGBT module, specially a single pack module..

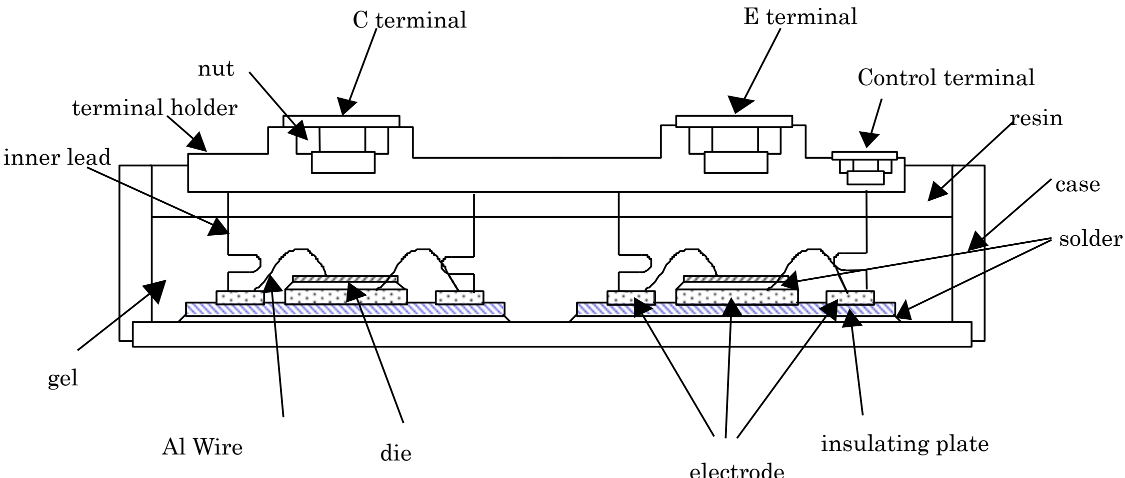
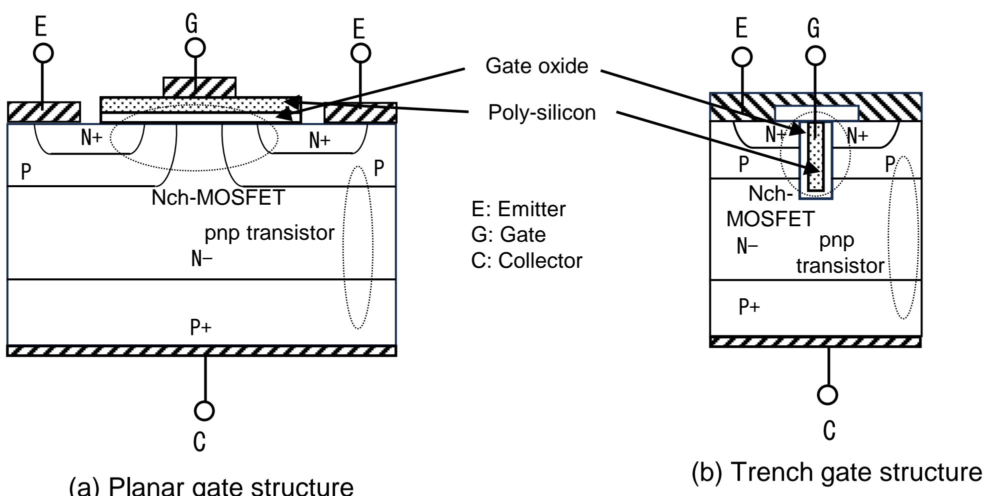


Figure 1.1 Schematic cross-section of the IGBT module.

1-4. IGBT structure

Figure 1.2 shows a schematic cross-section of the IGBTs. The IGBT structure is very similar to that of a power MOSFET (n-channel). Both IGBT and power MOSFET have a Nch-MOSFET region on the surface side. There are two types of Nch-MOSFET structures: planar and trench gate. The power MOSFET has an N^-/N^+ structure in the vertical direction. In contrast, the IGBT has an N^-/P^+ structure which forms a pnp transistor.



(a) Planar gate structure

(b) Trench gate structure

Figure1.2 Schematic cross-section of the IGBTs

1-5. Equivalent circuit and operating principle of the IGBT

1-5-1. Equivalent circuit of IGBT

Figure 1.3 shows the symbol and the equivalent circuit of the IGBT. In the equivalent circuit, the base-emitter resistance(r_b) of the npn transistor is designed to be very small to prevent the occurrence of latch-up phenomenon by malfunction of the npn transistor. In an IGBT module, diode is usually connected to IGBT in parallel, and in this case, the diode symbol is connected in parallel with the IGBT.

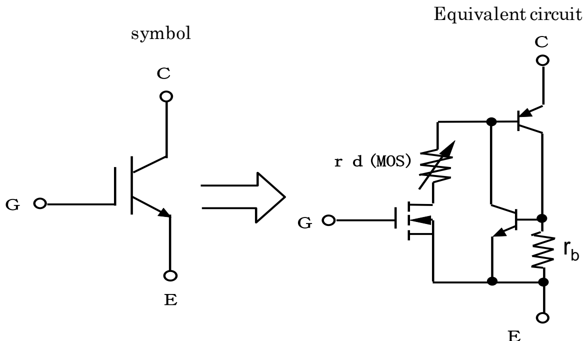


Figure1.3 IGBT symbol and equivalent circuit

1-5-2. Operating principle of the IGBT

Figure 1.4 shows the operating principle of the IGBT. MOSFET is turned on by first applying a voltage to gate-emitter electrode. As a consequence, the MOSFET's drain current flows as the base current of the pnp transistor. This base current turns on the pnp transistor, and the IGBT reaches its ON state. When the gate-emitter voltage becomes below the Gate-Emitter Threshold (a zero or minus biased), the MOSFET's current and the base current of the pnp transistor will be cut off, thus causing the IGBT to reach an OFF state. Since the IGBT is a composite device of a MOSFET and a pnp transistor, making them into a single chip can significantly reduce the resistance during current conduction by a phenomenon called “conductivity modulation”.

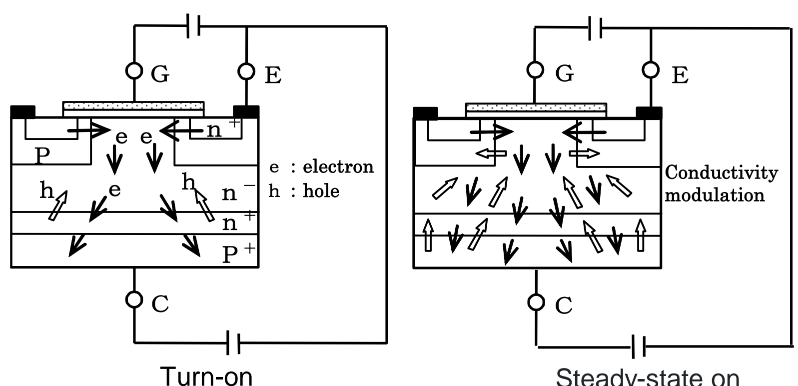


Figure1.4 Operating principle of the IGBT

1-5-3. IGBT device technology

Figure 1.5 shows a cross-sectional schematic diagram of the conventional trench gate structure and the side gate structure IGBT developed to reduce losses. In the side gate structure, a wider trench is formed compared to the conventional IGBT. This reduces the feedback capacitance "Cres", which enables fast switching and reduces losses. Figure 1.6 shows the trade-off improvement between the on-voltage $V_{CE(sat)}$ and turn-off loss E_{off} in a 3.3kV-rated IGBT. A 25% reduction in $V_{CE(sat)}$ was achieved when compared at the same E_{off}.

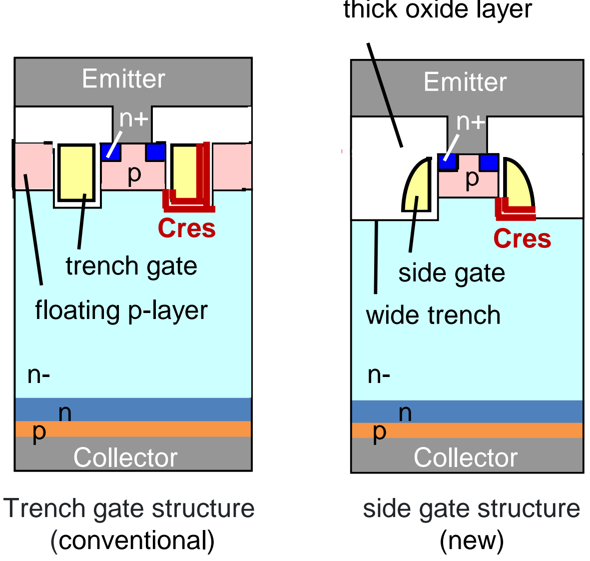


Figure1.5 Cross-sectional schematic diagram of the conventional trench gate structure and the side gate structure IGBT

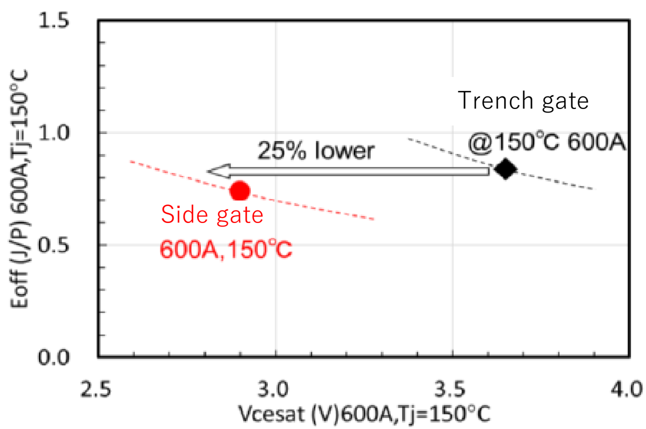


Figure1.6 Trade-off between $V_{CE(sat)}$ and turn-off loss E_{off}

2. Items listed on the specification sheet

Caution

●When designing electronic circuits using semiconductor devices, ensure that the specified "absolute maximum ratings" of the device are not exceeded under any external condition variations during operation. Additionally, for pulse applications, ensure that the ratings of the "safe operating area (RBSOA・RRSOA)" are not exceeded.

2-1. Example of the specifications

An example of the specifications in following Table 2.1

A) Absolute Maximum Ratings (Table 2.1, item ①)
Absolute maximum ratings apply to electrical, mechanical and thermal conditions that must be adhered to in order to prevent IGBT module destruction. Such conditions are generally expressed in terms of the maximum or minimum parameter values or to regions of Safe Operation Area (SOA). (If the module operates outside the listed scopes, it may break down.)

B) Electrical Characteristics (Table 2.1, item ②)
The electrical characteristics for IGBT module are set under certain measurement condition and its outcome is expressed in maximum, typical, and minimum values. These values are divided into three main characteristics; which are static characteristic, dynamic (switching) characteristic, and thermal characteristic.

C) Other cautions and notes (Table 2.1, items ③ and ④)
Precautions on the maximum rating and other matters are listed.

Table 2.1 Specification example(MBM450FS33F).

IGBT MODULE Spec.No.IGBT-SP-14035 R7 P1

MBM450FS33F

Module type

Specification control No.

Silicon N-channel IGBT 3300V F version

FEATURES

* High current density package
* Low stray inductance & low Rth(j-c)
* Half-bridge (2in1)
* Built in temperature sensor
* Scalable large current easily handled by paralleling
* Equipped with current sensing terminals

C1, C1AUX, G1, E1AUX, C2E1, C2AUX, G2, E2AUX, T, E2main, E2

Circuit diagram

ABSOLUTE MAXIMUM RATINGS (Tc=25°C)

Item		Symbol	Unit	MBM450FS33F
Collector Emitter Voltage		V_{CES}	V	3,300
Gate Emitter Voltage		V_{GES}	V	±20
Collector Current	DC	I_C	A	450
	1ms	I_{CM}		900
Forward Current	DC	I_F	A	450
	1ms	I_{FM}		900
Junction Temperature		$T_{vj\ op}$	°C	-50 ~ +150
Storage Temperature		T_{stg}	°C	-55 ~ +150
Isolation Voltage		V_{ISO}	V_{RMS}	6,000(AC 1 minute)
Screw Torque	Terminals (M3/M8)	M	N·m	0.8/15
	Mounting (M6)	M		6.0 (1)

①

Notes: (1) Recommended Value 5.5±0.5N·m

③

Table 2.1 Specification example(MBM450FS33F).

ELECTRICAL CHARACTERISTICS

Item		Symbol	Unit	Min.	Typ.	Max.	Test Conditions
Collector Emitter Cut-Off Current		I_{CES}	mA	-	-	0.30	V_{CE}=3,300V, V_{GE}=0V, T_{vj}=25°C
				-	15	50	V_{CE}=3,300V, V_{GE}=0V, T_{vj}=150°C
Gate Emitter Leakage Current		I_{GES}	nA	-500	-	+500	V_{GE}=±20V, V_{CE}=0V, T_{vj}=25°C
Collector Emitter Saturation Voltage		V_{CEsat}	V	-	2.25	-	I_C=450A, V_{GE}=15V, T_{vj}=25°C
				2.50	3.05	3.50	I_C=450A, V_{GE}=15V, T_{vj}=150°C
Gate Emitter Threshold Voltage		$V_{GE(th)}$	V	5.5	6.5	7.5	V_{CE}=10V, I_C=450mA, T_{vj}=25°C
Input Capacitance		C_{ies}	nF	-	24	-	V_{CE}=10V, V_{GE}=0V, f=100kHz, T_{vj}=25°C
Internal Gate Resistance		$R_{G(int)}$	Ω	-	6.2	-	V_{CE}=10V, V_{GE}=0V, f=100kHz, T_{vj}=25°C
Turn On Delay Time		$t_{d(on)}$	µs	-	0.48	-	V_{CC}=1800V, I_C=450A
Rise Time		t_r		-	0.12	-	Ls=40nH
Turn Off Delay Time		$t_{d(off)}$		-	1.10	-	R_G(on/off)=6.8Ω/12Ω (2)
Fall Time		t_f		-	1.30	-	V_{GE}=±15V, T_{vj}=150°C
Forward Voltage Drop		V_F	V	-	2.25	-	I_F=450A, V_{GE}=0V, T_{vj}=25°C
				2.10	2.45	2.80	I_F=450A, V_{GE}=0V, T_{vj}=150°C
Reverse Recovery Time		t_{rr}	µs	-	1.10	-	V_{CC}=1800V, I_F=450A, Ls =40nH T_{vj}=150°C
Turn-on Loss per Pulse		E_{on}	J/P	-	0.73	-	V_{CC}=1800V, Ic=450A, Ls =40nH
Turn-off Loss per Pulse		E_{off}	J/P	-	0.63	-	R_G(on/off)=6.8Ω/12Ω (2)
Reverse Recovery Loss per Pulse		E_{rr}	J/P	-	0.68	-	V_{GE}=±15V, T_{vj}=150°C
Short Circuit Pulse Width		t_{sc}	µs	10	-	-	Vcc=2200V,Ls=40nH R_G(on/off)=6.8/68Ω, V_{GE}=±15V,Tvj=150℃
Stray Inductance Module		L_{SCE}	nH	-	9	-	Between C1(main) and E2(main)
NTC-Thermistor	Resistance	R_{25}	kΩ	-	5	-	Tc=25 °C
	Deviation	ΔR/R	%	-5		5	Tc=25 °C
	B-constant	$B_{(25/50)}$	K	-	3375	-	Between 25℃ and 50℃
Thermal Impedance	IGBT	Rth(j-c)	K/W	-	-	0.035	Junction to case
	FWD	Rth(j-c)		-	-	0.055	
Contact Thermal Impedance		Rth(c-f)	K/W	-	0.02	-	Case to fin (per 1 arm)

②

Notes: (2) R_G value is a test condition value for evaluation, not recommended value.
Please determine the suitable R_G value by measuring switching behavior and checking results with the respective SOA.

* Please contact our representatives at order. * For improvement, specifications are subject to change without notice.
* For actual application, please confirm this spec sheet is the newest revision.
* ELECTRICAL CHARACTERISTIC items shown in above table are according to IEC 60747–2 and IEC 60747–9.

④

2-2. Technical term

The terms used in specifications and other documents in the following.

Table 2.2 Maximum ratings

TERMS		SYMBOLS	DEFINITIONS
Collector Emitter voltage		V_{CES}	Maximum Collector-Emitter (hereinafter called C-E) voltage with Gate-Emitter (G-E) shorted
Gate Emitter voltage		V_{GES}	Maximum G-E voltage with C-E shorted
Collector current		I_C	Maximum DC collector current of IGBT
		I_{CRM}	Maximum pulse collector current of IGBT
Forward current		I_F	Maximum DC forward current of FWD(Freewheeling Diode)
		I_{FRM}	Maximum pulse forward current of FWD
I^2t		I^2t	Joule integral of the overcurrent allowed by the diode commercial sine half-wave (50, 60 Hz), specified in 1 cycle
Maximum junction temperature		T_{Vjmax}	Temperature at which the device can operate without causing malfunction
Operating junction temperature		T_{vjop}	Temperature at which the device can be operated continuously
Storage Temperature		T_{stg}	Range of allowable temperature for storage of IGBT module without electric load
Isolation voltage		V_{ISO}	The maximum allowable sinusoidal voltage RMS value between the electrodes and the heat sink mounting surface when all electrodes of the IGBT module are shorted.
Screw Torque	Terminals	-	Maximum allowable value of clamping torque when attaching wiring materials, etc. to the terminals with the specified screws, bolts, etc.
	Mounting	-	Maximum allowable value of clamping torque when IGBT module is mounted onto heat sink or support, using specified grease on screw and contact portions.
	PCB Mounting	-	Maximum allowable value of clamping torque when the PCB board mounted onto the IGBT module, using specified bolts.

2-3. Electrical characteristics

Table 2.3 Static electrical characteristics

Term	Symbol	Definition
Collector cut-off current	I_{CES}	Collector leakage current flowing through C-E with G-E shorted and the specified voltage between C-E
Gate Emitter leakage current	I_{GES}	Gate leakage current flowing through G-E with the specified voltage between G-E
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	G-E voltage at a specified C-E voltage and collector current when collector current starts to flow (in threshold region)
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	C-E voltage at a specified collector current and G-E voltage.
Input capacitance	C_{ies}	G-E capacitance when a specified voltage is applied between G-E and C-E while C-E is shorted in AC.
Output capacitance	C_{oes}	C-E capacitance when a specified voltage is applied between G-E and C-E while G-E is shorted in AC.
Reverse transfer capacitance	C_{res}	C-G capacitance when a specified voltage is applied between G-E and C-E while G-E and C-E are shorted in AC.
Forward voltage drop (Diode)	V_F	Forward voltage of diode at a specified forward current.
Internal gate resistance	r_g	Gate series resistance built into IGBT modules
Gate charge	Q_g	Total charge between given gate voltages
Stray inductance	L_{SCE}	Stray inductance of IGBT modules

Table 2.4 Dynamic electrical characteristics

Term	Symbol	Definition
Turn-on Delay Time	$t_{d(on)}$	The time from when the gate voltage reaches 10% of the maximum forward bias value the collector current reaches 90% of the set value.
Rise Time	t_r	Time required collector current to reach 10% to 90% of its initial value.
Turn-on Time[*1]	ton	(1) IEC standard :$td_{(on)}$+tr (2) Under specified conditions, time required for collector-emitter voltage to reach 10% of its initial value after the moment when ON-gate voltage has reached 10% of its final value and through the subsequent switching of IGBT module from OFF state to ON state
Turn-off Delay Time	$t_{d(off)}$	Time required for collector current to reach 90% of its initial value after the moment when OFF-gate voltage has reach 90% of its initial value.
Fall Time	t_f	Time required for collector current to reach 90% from 10% of its initial value.
Reverse Recovery Time (Diode)	t_{rr}	Time required for reverse recovery current of the diode to vanish, under specified circuit and temperature conditions.
Turn-on loss	E_{on}	Loss generated during IGBT turn-on.
Turn-off loss	E_{off}	Loss generated during IGBT turn-off.
Short circuit current	I_{SC}	Maximum current during short circuit
Reverse recovery loss	E_{rr}	Loss generated during FWD reverse recovery

Note *1: Please refer to the data sheet for the definition of (1) or (2).

Table 2.5 Thermal characteristics

Term	Symbol	Definition
Thermal resistance characteristics	$R_{th(j-c)}$	Under thermal steady-state while IGBT module is continuously energized, value of temperature difference between junction and case per unit power dissipation at junction.
	$R_{th(c-f)}$	Under thermal steady-state while IGBT module is continuously energized, value of temperature difference between junction and heatsink(fin) per unit power dissipation at junction when the IGBT module is attached to the heat sink using thermal grease at the recommended torque value.
	$R_{th(f-a)}$	Value of temperature difference between heatsink(fin) and ambient heatsink(fin) per unit power dissipation

Table 2.6 Thermistor characteristics

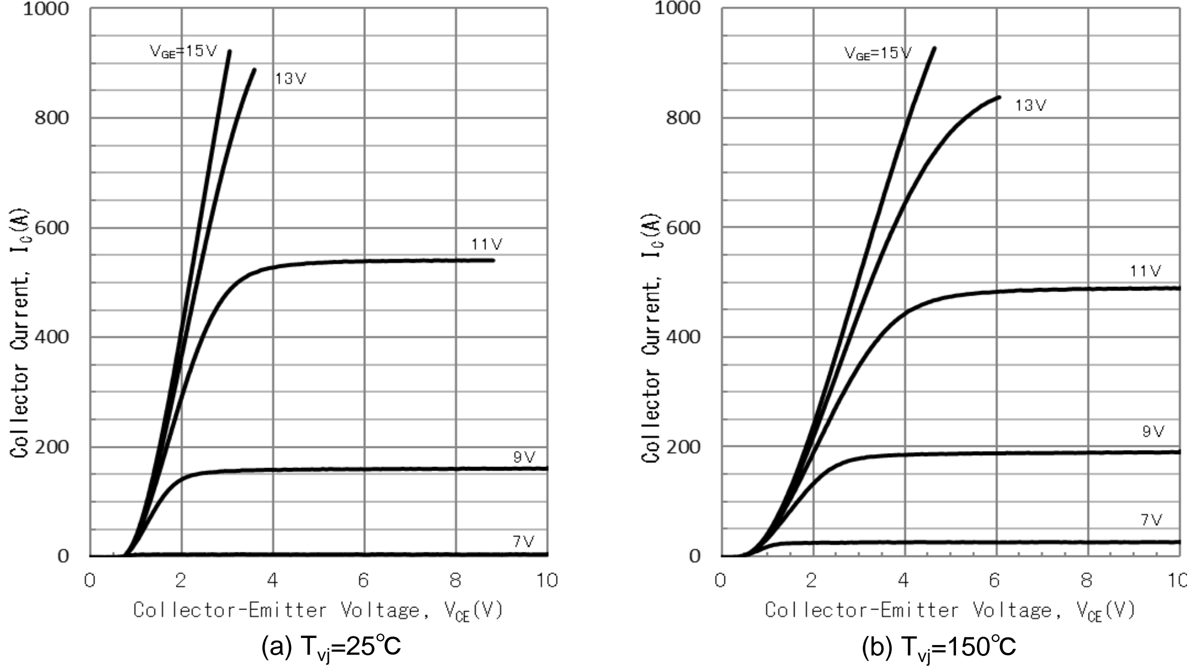
Term	Symbol	Definition
Thermistor resistance	R	Thermistor resistance at specified temperature
Thermistor leakage current	-	Leakage current between the thermistor terminals and other terminals at a specified voltage when terminals other than the thermistor are shorted.

2-4. Characteristics Curves of the IGBT module

Taking the 3.3 kV/450 A 2-in-1 IGBT module MBM450FS33F as an example, the typical characteristic items, contents and purpose of use are shown as follows.

2-4-1. Static characteristics

(1) The collector current vs. collector-emitter voltage characteristics (V_{CE}-I_C characteristics) represents the relationship between the collector-emitter voltage and collector current as a function of the gate-emitter voltage. These characteristics are used to calculate the conduction losses of the IGBT. Figure 2.1(a) shows the V_{CE}-I_C characteristics at T_j=25℃, and (b) shows the characteristics at T_j=150℃. At low currents, the collector voltage V_{CE} decreases with increasing temperature. Conversely, at high currents, V_{CE} increases increasing temperature. It is important to consider these characteristics for thermal design.



(a) T_{vj}=25℃ (b) T_{vj}=150℃

Figure2.1 Collector Current vs. Collector-Emitter Voltage Characteristics (V_{CE}-I_C Characteristics): Typical

(2) Capacitance Characteristics

Figure 2.2 shows the gate charge (V_{GE}-Q_g) characteristics. The V_{GE}-Q_g characteristics indicate the amount of charge required to drive the IGBT and are used to determine the power supply capacity of the driver circuit. The method for calculating the losses of the driver circuit using this graph will be explained in Chapter 3. Additionally, the collector-emitter voltage dependency of the parasitic capacitances of the IGBT, including the input capacitance Cies, output capacitance Coes, and feedback capacitance Cres, are shown in Figure 2.3. These characteristics should be used for designing drive circuits, especially dead time setting.

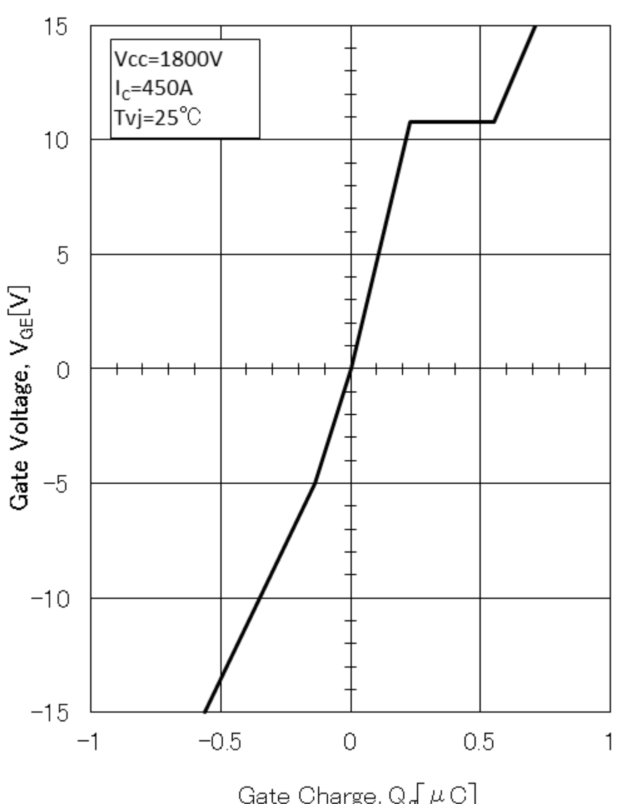


Figure2.2 Gate Charge Characteristics (V_{GE}-Q_g): Typical

Collector

C_{GC}

C_{CE}

Gate

C_{GE}

Emitter

$C_{ies}=C_{GE}+C_{GC}$
$C_{oes}=C_{CE}+C_{GC}$
$C_{res}=C_{gc}$

Figure2.3 IGBT parasitic capacitance

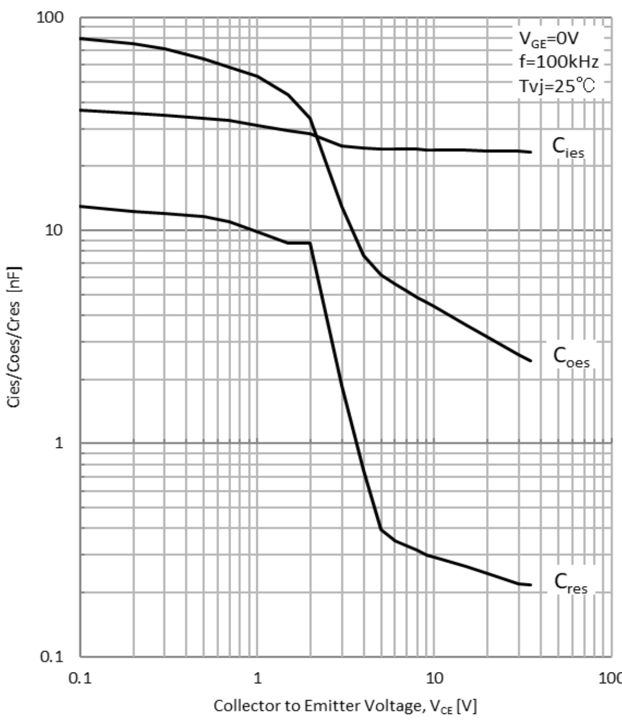


Figure2.4 Dependence of parasitic capacitance on collector-emitter voltage：Typical

(3) Diode forward voltage characteristics （V_F-I_F characteristics ）

The VF-IF characteristics represents the relationship between the forward voltage (VF) and forward current (IF) of the diode (FWD) connected in parallel with the IGBT. These characteristics are used to calculate the conduction loss of the FWD. Figure 2.5 shows the VF-IF characteristics at Tj=25℃ and 150℃. Similar to the IGBT, the forward voltage VF decreases with increasing temperature at low currents. Conversely, at high currents, VF increases with increasing temperature. Therefore, it is important to consider these characteristics for thermal design, just as with the IGBT.

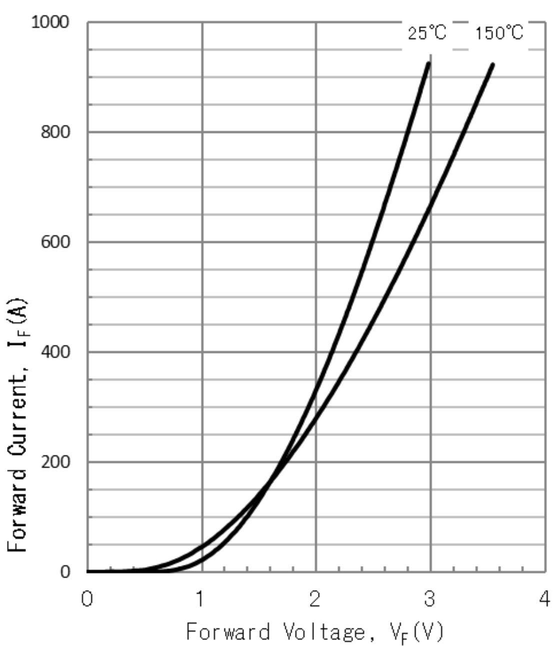


Figure2.5 Forward characteristics of Diode

(4) Temperature Dependence of Maximum Collector-Emitter Voltage

At lower temperatures, the breakdown voltage between the collector and emitter decreases. Therefore, it is important to verify the surge voltage during switching tests at the lowest operating temperature. The breakdown voltage of the IGBT and diode is designed to higher than the maximum collector-emitter voltage at the minimum junction temperature. Consequently, the specification sheet indicates a constant maximum collector-emitter voltage across the entire range from the minimum to the maximum junction temperature. However, some products exhibit a decrease in the maximum collector-emitter voltage at lower temperatures, so please refer to the specification sheet for each product.

2-4-2. Switching characteristics

The switching characteristics of the IGBT during turn-on and turn-off are influenced by various parameters such as the current I_C, junction temperature T_{vj}, gate voltage V_{GE}, and gate resistance R_g. Additionally, these characteristics are also affected by wiring and layout. Therefore, it is strongly recommended to measure the switching characteristics using the actual equipment. Switching characteristics is divided into two categories: switching time and switching losses. These switching characteristics can be measured using the half-bridge shown in Figure 2.6. The definitions of the dynamic characteristics items listed in Table 2.4, including td(on), tr, ton, td(off), tf, Eon, Eoff, and Err, are illustrated in Figure 2.7.

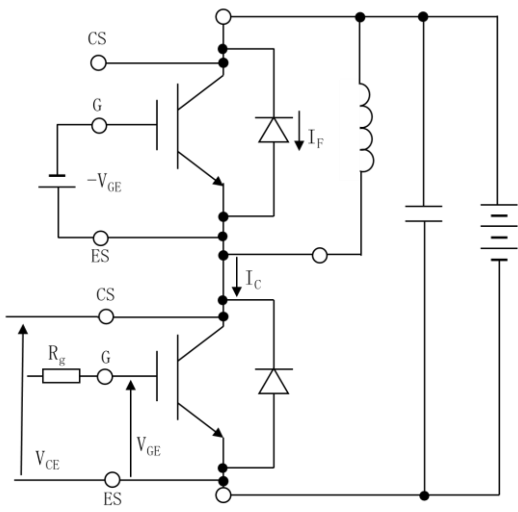


Figure2.6 Switching Characteristics Evaluation Circuit (Half-bridge)

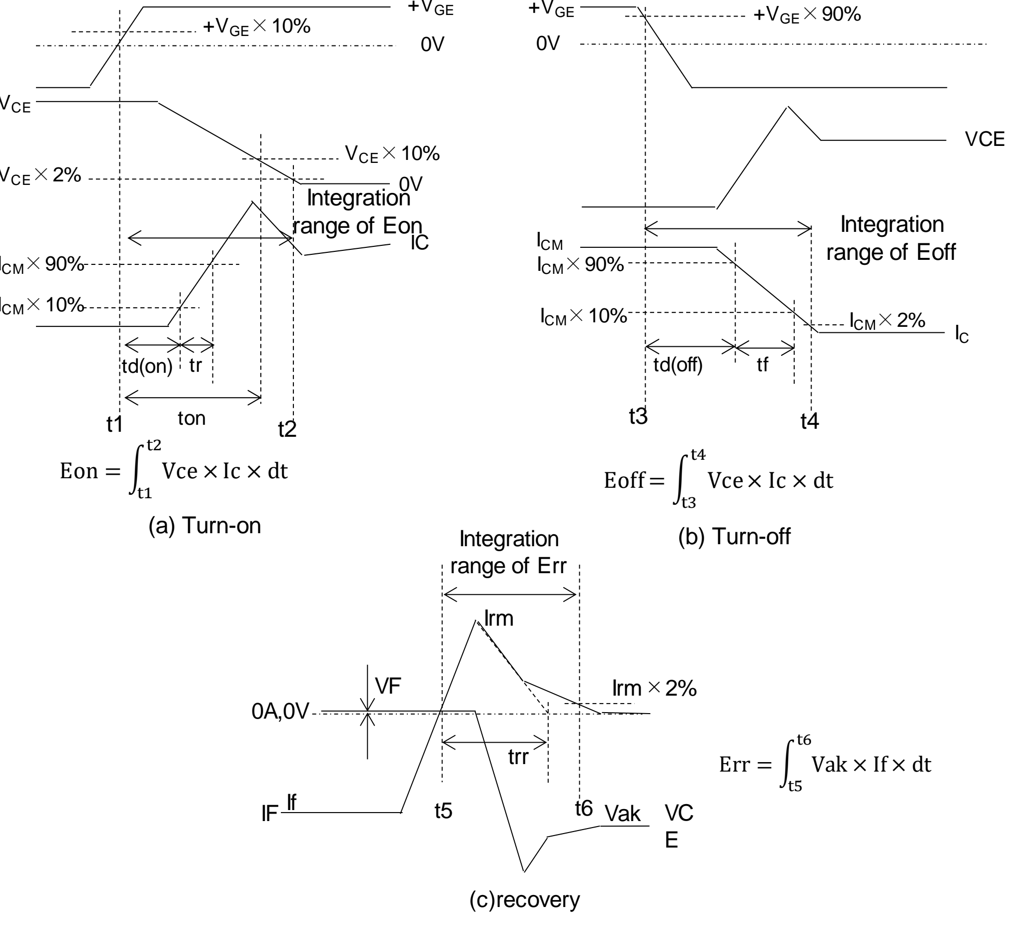


Figure2.7 Definition of Switching Characteristics

Figure 2.8 show the collector current I_C dependency of the switching time and Figure 2.9 shows that of the gate resistance R_g dependency. As shown in these figures, the switching time varies with I_C and R_g, so please consider these characteristics for designing the equipment.

For example, operation with insufficient dead time due to long switching times may lead to short-circuiting of the upper and lower arms, increasing losses and is possible to cause device failure. Additionally, in cases of shorter switching times, particularly short tr and tf, a high transient current change rate (di/dt) may occur and this causes the surge voltage Ls×di/dt due to the stray inductance Ls. This surge voltage is superimposed on the DC voltage and has the possibility to cause deviation of the SOA and failure of IGBT.

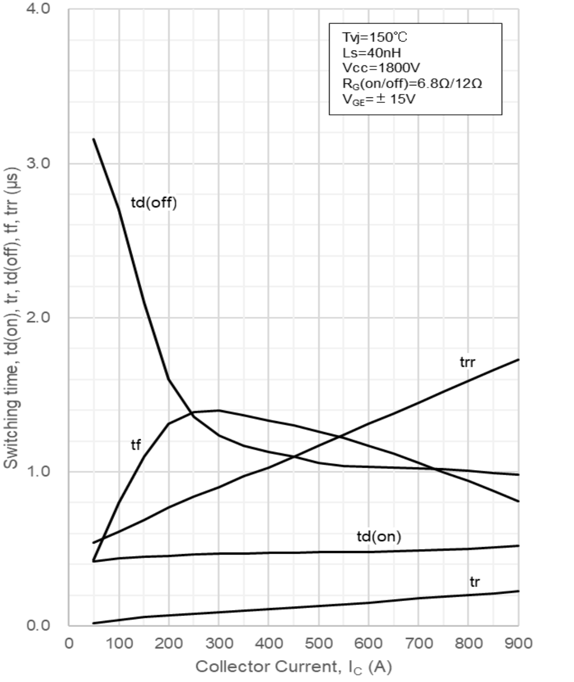


Figure2.8 Switching times - I_C characteristics : Typical

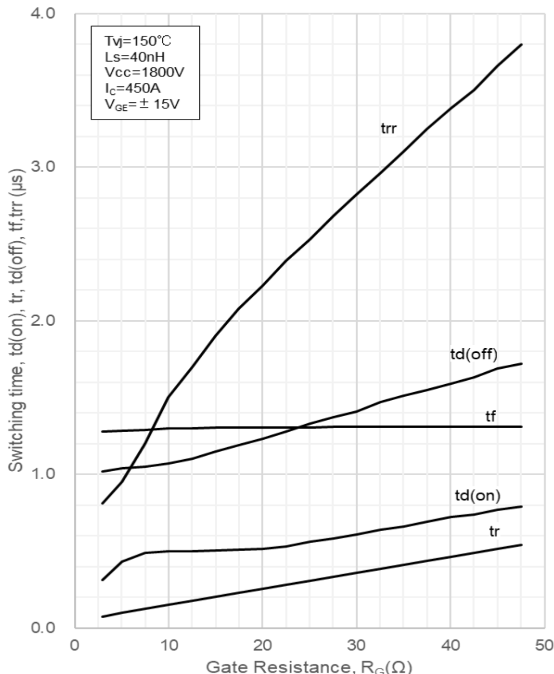


Figure2.9 Switching times - R_g characteristics : Typical

The turn-on loss (Eon) and turn-off loss (Eoff) occur during the IGBT's switching process, while the recovery loss(Err) occurs when the diode is recovered. Both IGBT and diode losses increase with increasing temperature. Figure 2.10 shows the collector current I_C dependency of the switching losses. Switching losses increase with increasing Ic. Figure 2.11 shows the gate resistance Rg dependency of the switching losses. Lower Rg results in reduced IGBT switching losses, particularly the turn-on loss. However, because the switching times tr and tf become shorter, the transient current change rate (di/dt) increases and a larger surge voltage Ls×di/dt due to the stray inductance Ls may be occurred.

The stray inductance of the circuit includes not only the stray inductance of the power module but also the sum of the inductance of the smoothing capacitor and the wiring (bus bar) between the smoothing capacitor and the power module. Therefore, for determining Rg, it is necessary to evaluate the switching characteristics using the smoothing capacitor, bus bar, and gate circuit used in the real equipment.

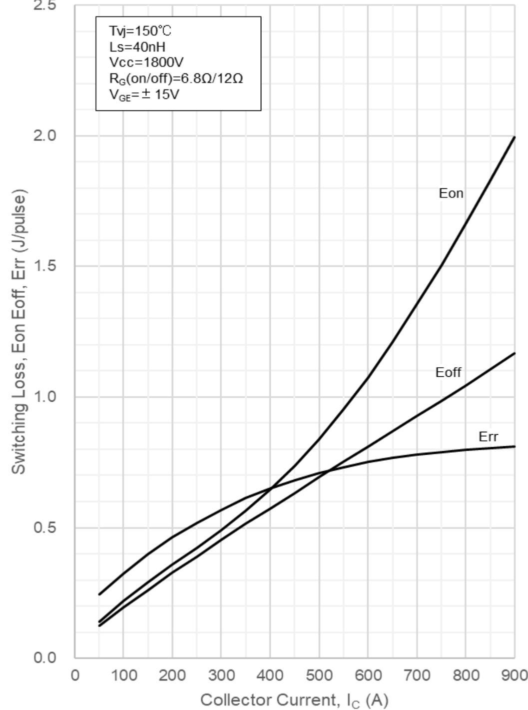


Figure 2.10 Switching losses - I_C characteristics : Typical

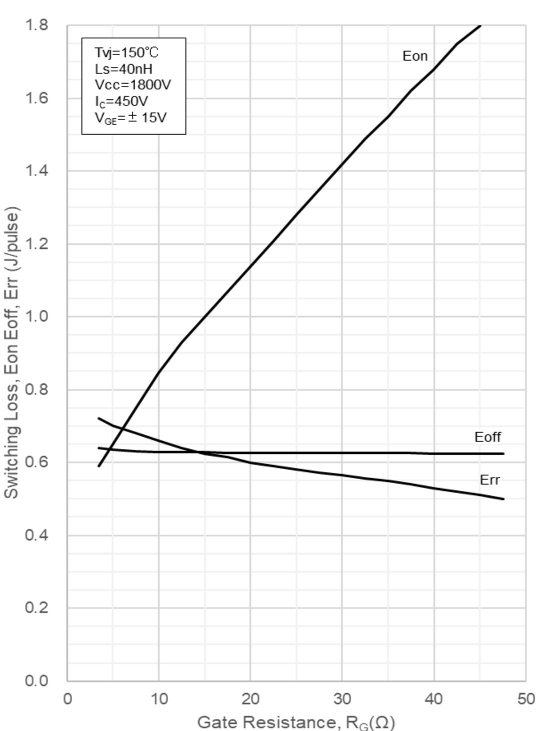


Figure 2.11 Switching losses - R_g characteristics : Typical

2-4-3. Reverse Bias Safe Operating Area(RBSOA)

IGBT can be safely turned off within the reverse bias safe operating area (RBSOA), which represents the collector voltage (V_{CE}) and collector current (I_C) operating range for safe turn-off. An example for the MBM450FS33F is shown in Figure 2.12.

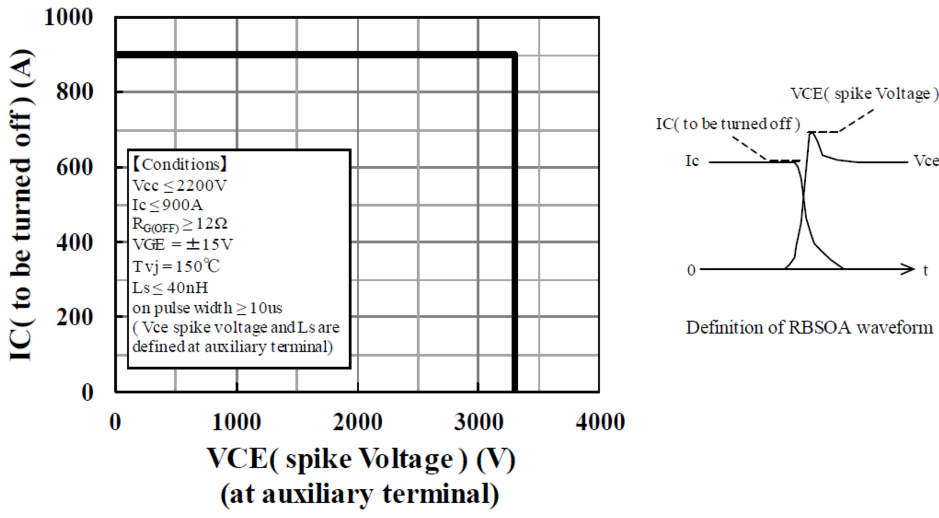


Figure2.12 Reverse Bias Safe Operating Area (RBSOA)

: Typical

2-4-4. Reverse Recovery SOA (RRSOA)

Similar to RBSOA of the IGBT, diodes also have a Safe Operating Area (SOA). The SOA for diodes is called the Reverse Recovery SOA (RRSOA), and it represents the area and power which the diode can be recovered without failure. An example is shown in Figure 2.13.

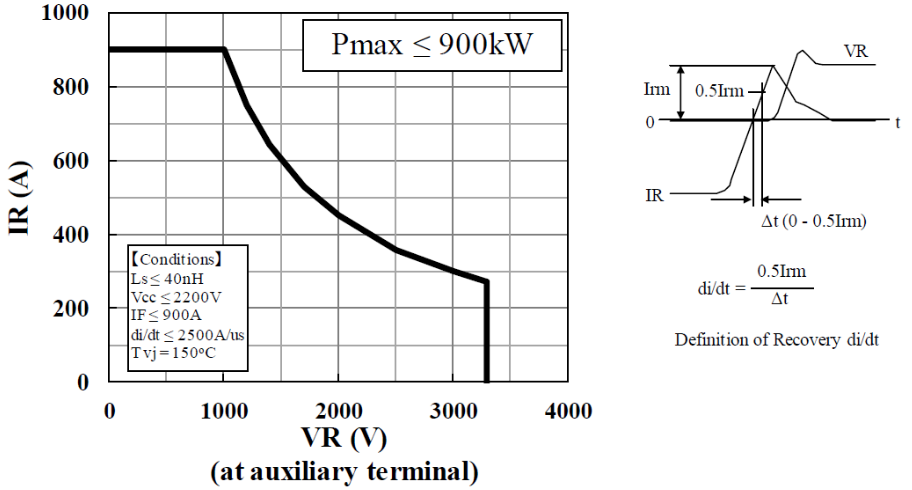


Figure2.13 Reverse Recovery SOA(RRSOA)

: Typical

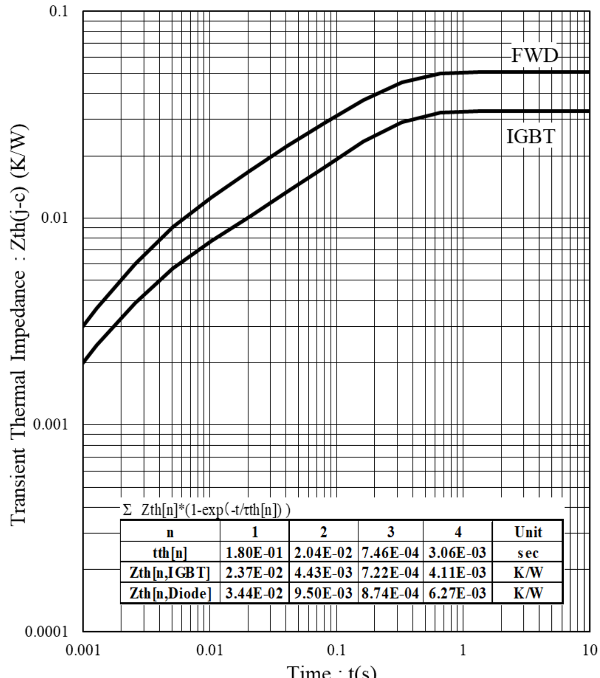
2-4-5. Transient Thermal Resistance

The transient thermal resistance characteristics used to calculate the temperature rise of IGBTs and diodes are shown in Figure 2.14.

Using the transient thermal resistance, the temperature difference ΔT (K) is defined as:

ΔT (K) = Thermal Resistance(K/W) × Loss (W)

Details will be explained in Chapter 3.



n	1	2	3	4	Unit
tth[n]	1.80E-01	2.04E-02	7.46E-04	3.06E-03	sec
Zth[n,IGBT]	2.37E-02	4.43E-03	7.22E-04	4.11E-03	K/W
Zth[n,Diode]	3.44E-02	9.50E-03	8.74E-04	6.27E-03	K/W

Fig2.14 Transient Thermal Resistance : Typical

3. Precautions for Safe Use

3-1. Derating

To ensure IGBT module reliability, please follow each of derating listed below.

Although a three-phase inverter will be used as an example here, the idea of derating can also be used in other applications.

(1) Voltage：Maximum peak voltage should not exceed 80% of rated voltage VCES, and the DC voltage should not exceed 50 to 60% of VCES.

At maximum peak (non-steady-state), VCES is under 90% (peak voltage value).

Note: Use Equation (1) to calculate the rated voltage of an IGBT module for a given AC line input voltage at the inverter.

$$V_{CES} = Vin \times \sqrt{2} + V_s + V_{reg} + \alpha \quad ---(1)$$

V_{CES} ; Rated Voltage

V_{in} ; Input Voltage (AC voltage)

V_s ; Surge Voltage (Peak Voltage)

V_{reg} ; Increase in DC voltage due to regenerative braking, etc.

α ; Margin , Safety factor

(2) Current：Current: During the steady-state condition, IGBT module DC current should not exceed 50 to 60% of the rated DC current (repetitive current peak value).

Maximum value (non-steady-state) should not exceed 90% of the rated DC current (repetitive current peak value). However, if derating at the junction temperature, current is derated accordingly. In addition, 1ms rated current (Icp) in the specifications is the peak current value including recovery current (a few μs or less) during reverse recovery of the free-wheeling diode, and are intended to serve as protection against accidents such as load short-circuits.

In particular, this value cannot be used repeatedly during faults such as load short circuit protection that leaves thermal history. Selection of the rated DC current (rated collector current) of IGBT module that takes into account derating can be considered by using the following equation.

$$I_p = P_{inv} \times \kappa \div V_{ac} \div \sqrt{3} \times \sqrt{2} \times \lambda \quad ---(2)$$

$$I_c > Ip \div \beta \quad ---(3)$$

I_p ; Peak current

P_{inv} ; Capacity of inverter

K ; Overload ratio

V_{ac} ; AC voltege

λ ; Current ripple ratio

I_C ; Rated DC current (Collector current rating)

β ; Derating factor

(3) Junction temperature: During the steady-state condition, below 80% of the rated junction temperature (maximum value). Maximum (non-steady state) condition, the junction temperature should be no more than 90% of the rated maximum.

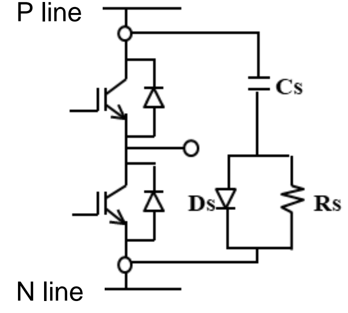
Case temperature should not exceed 100℃. In addition, repetitive change in junction temperature Tj and case temperature Tc causes stress to internal parts of the module, and depending on how frequently they are changed, it may reduce the life of the device, so please be careful. For more details, please refer to Section 3-7 "Thermal Resistance and Heat Dissipation Design".

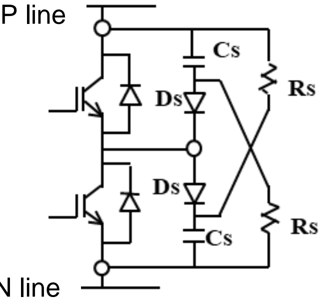
3-2. Snubber Circuit

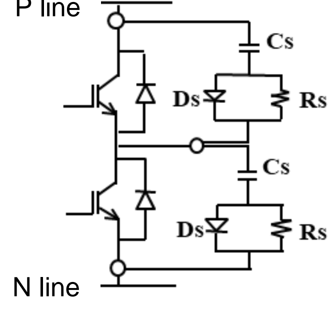
The snubber circuit is a circuit inserted to protect the switching device (when the switching device is turned OFF) from the surge voltage generated by the charged energy in the line inductance. There are generally two types: a non-polar type consisting of C and R and a polar type with an added diode. With the IGBT, the polar type with high voltage surge suppression is used. In addition, the IGBT may be used without the snubber circuit if the main circuit line inductance is greatly reduced and the peak surge voltage can be controlled to about 80% or less of the IGBT module's maximum rating.

3-2-1. Types and characteristics of snubber circuits

Figure 3.1 show the types and characteristics of snubber circuits.







The capacitor Cs is constantly applied with the BUS voltage, and it suppresses surge voltage. The arrangement of Ds, Rs, and Cs is not restricted by this configuration. This type of snubber circuit is used for relatively small-capacity devices.	Both the upper and lower Cs are applied with the BUS voltage and each operate as suppression circuit for the upper and lower arms. This type of snubber circuit is used for relatively high current capacity devices.	For each arm's switching, Cs repletely is charged and discharged between 0V and the BUS voltage. This results in significant snubber circuit losses. This type of snubber circuit is often used for devices with narrow SOA, such as GTOs.

Figure3.1 Types and characteristics of snubber circuits

3-2-2. Operation of Snubber circuits

Figure 3.2 shows the circuit representing the overvoltage generation mode during the turn-off of the lower arm IGBT, and Figure 3.3 shows the equivalent circuit of the transient state at that time.

The current loop path due to the turn-off of the lower arm IGBT.

The current path during the conduction of the lower arm IGBT.

Lst Eo C IGBT IGBT Lsn FWD Cs IGBT LOAD FWD Ds Rs

Figure3.2 Turn-off mode of the lower arm IGBT

Lst Lsn Eo C FWD Cs Ds Rs

Figure3.3 The equivalent circuit of the transient state in the Figure3.2

Figure 3.3 shows the change in current path when the lower arm IGBT, which was previously on, is turned off. When the lower arm IGBT is turned off, the load current flows through the upper arm's FWD. Without a snubber circuit, because there is no designated circuit which can consume the stored energy in Lst, this energy would cause the surge voltage of the lower arm IGBT. By applying a snubber circuit, as shown in Figure 3.3, the storage energy in Lst is consumed by the snubber capacitor Cs and change to the voltage. This operation serves to suppress surge voltage caused by Lst. However, in reality, the snubber circuit also has wiring stray inductance Lsn, which leads to some surge voltage at the turn-off of the IGBT.

3-2-3. The current and voltage waveforms when using a snubber circuit.

In the circuit shown in Figure 3.2, Figure 3.4 shows the current and voltage waveforms of the IGBT at turn-off. The use of a snubber circuit suppresses the surge voltage caused by the wiring stray inductance Lst to Eo + ΔV.

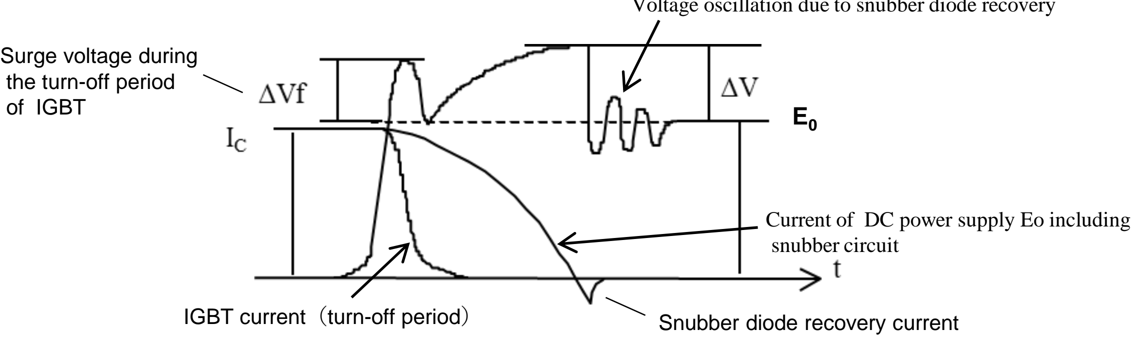


Figure3.4 The IGBT current (I_C) and voltage (V_{CE}) waveforms with a snubber circuit

Figure 3.5 shows the current (iDs) and voltage (vDs) waveforms of the snubber diode Ds at turn off of the IGBT. Each parameter can be approximately calculated using the following equations:

$$Ts = \frac{2\pi\sqrt{Lst \times Cs}}{4} \quad ---(4)$$

$$\Delta V = IC \times \sqrt{\frac{Lst}{Cs}} \quad ---(5)$$

where (I_C) is the IGBT turn-off current value.

$$\Delta Vf = Lsn \times dic/dt + Vfr \quad ---(6)$$

Here, (Lsn) is the stray inductance value of the snubber circuit from the collector-emitter terminals of the IGBT, (Vfr) is the forward recovery voltage of the diode (approximately 50V), and dic/dt is the rate of current change during the turn-off period.

$$Tn \fallingdotseq 3 \times Cs \times Rs \quad ---(7)$$

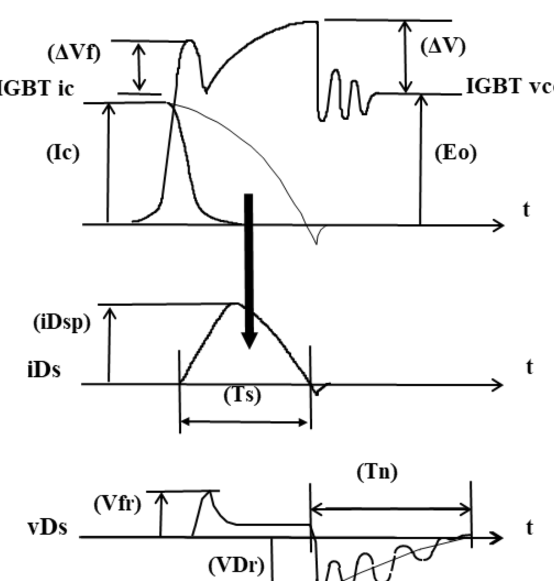


Figure3.5 Waveforms of each part of the snubber circuit

Here, Tn represents the time required to discharge 95% of the overcharged voltage of Cs. Additionally, Rs is selected to satisfy the condition $Ts + Tn < 1/fc$. In the case of a three-phase circuit, for the Eq.s (4), Ts becomes $\sqrt{3}$ times, and for the Eq.(5), ΔV becomes $1/\sqrt{3}$ times (the snubber circuit also works for other phases).

3-2-4. The collector current class and snubber capacitor capacity

Assuming the maximum switching current value as I and the voltage rise as ΔV, the snubber circuit capacitance, Cs can be calculated as follows:

$$Cs \fallingdotseq Lst \times \left(\frac{I}{\Delta V}\right)^2 \quad ---(8)$$

・Please use a polyester film capacitor with good frequency characteristics for the snubber capacitor.

・Note the thickness of the capacitor leads because charging and discharging currents may cause the lead wires to become hot with thin wires, which may exceed the heat resistance of the capacitor.

3-2-5. Snubber resistor

The capacity of the resistor varies depending on the capacity of the capacitor and the driving frequency of the IGBT. Using the overcharged voltage ΔV in the snubber, the energy ε_{SN} generated when the current I is turned off is as follows, and most of the energy is consumed by the snubber resistor.

$$\varepsilon_{SN} = 0.5 \times Cs \times \Delta V^2 \quad \text{---(9)}$$

The resistance value is determined by the following Eq.to prevent oscillation of the collector current when the IGBT is turned on.

$$Rs \geqq 2\sqrt{\frac{L_{sn}}{C_S}} \quad \text{---(10)}$$

L_{sn} : Stray inductance of the snubber wiring

Additionally, since Rs serves as the resistor to discharge the overcharged ΔV in Cs, note its upper limit. Depending on the carrier frequency, the voltage ΔV of Cs should be discharged as quickly as possible.

3-2-6. Snubber diode

The snubber diode should have a voltage rating equal to or greater than that of the IGBT, and its current capacity (or current rating) should be at least 1/10 ~ 1/5 of the IGBT's rating. The diode should be of a high-speed type. If the diode has a hard recovery characteristic, be cautious as it may cause high-frequency oscillations in the collector voltage during the IGBT's turn-off.

3-3. Gate Drive Circuit

The voltage and current waveforms during the switching of IGBTs and diodes vary depending on the gate forward bias ($+V_{GE}$), gate reverse bias ($-V_{GE}$), and gate resistance (R_g). Therefore, it is necessary to set these parameters according to the design objectives of the device. The following are the considerations for $+V_{GE}$, $-V_{GE}$, and R_g.

3-3-1. Gate forward bias : $+V_{GE}$

Recommended gate forward bias voltage $+V_{GE}$ is +15V.

(1) Design $+V_{GE}$ to be within the maximum gate-emitter voltage rating of 20V.

(2) It is recommended that the gate power supply voltage variation be within ±10%.

(3) The $_{VCE(sat)}$ during the on period decreases as $+V_{GE}$ increases, which means the steady-state losses decrease.

(4) The turn-on losses decrease as $+V_{GE}$ increases. However, the surge voltage during the recovery of the opposite (anti-parallel) arm diode increases.

(5) The turn-off losses are minimally affected if the gate power supply voltage variation is within ±10%.

(6) The short-circuit current increases as $+V_{GE}$ increases, which reduces the short-circuit withstand capability.

3-3-2. Gate reverse bias : $-V_{GE}$

The recommended value for the gate reverse bias voltage $-V_{GE}$ is between -5V and -15V.

(1) Design $|-V_{GE}|$ to be within the maximum gate-emitter voltage rating of 20V.

(2) It is recommended to keep the variation in the gate power supply voltage within ±10%.

(3) The larger the $-V_{GE}$, the shorter the turn-off time and the lower the turn-off losses. However, the surge voltage increases.

(4) The occurrence of dV/dt-induced false turn-on is more likely when $-V_{GE}$ is small.

3-3-3. Gate resistor : R_g

The R_g described in the specifications is the value that, under our measurement conditions, results in the lowest switching losses within the absolute maximum rating voltage and current at the recommended gate voltage.

(1) As R_g increases, the turn-on and turn-off delay times (td(on) and td(off)) become longer. The turn-on rise time (tr) also increases, and the recovery surge voltage of the diode decreases. The turn-off fall time(tf) depends on the device structure. Therefore, increasing R_g have possibility to an increase in the surge voltage during turn-off.

(2) Turn-on loss (Eon) increases with R_g. Turn-off loss (Eoff) also increases with larger R_g, but its dependency on R_g is smaller compared to Eon. Recovery loss decreases with R_g.

(3) Various switching characteristics are significantly affected by parasitic inductance in the circuit configuration. In particular, the surge voltage generated during IGBT turn-off and diode recovery is greatly influenced by stray inductance. Therefore, design R_g with the stray inductance of the circuit kept as small as possible.

3-3-4. Prevention for dV/dt-induced false turn-on during diode reverse recovery

Figure 3.6 explains the principle of false turn-on caused by dVCE/dt during diode recovery. When the lower arm IGBT2 is in the off state and the reverse current flows through the forward diode FWD1 of the upper arm IGBT1, and the lower arm IGBT2 transitions to the on state, FWD1 undergoes reverse recovery. At this time, the collector-emitter voltage V_{CE} of IGBT1 increases, causing dVCE/dt. This dVCE/dt causes a current I_G = Cres × dVCE/dt to flow into the gate through the reverse transfer capacitance of IGBT1. This current flowing into R_g causes the gate voltage V_{GE} of IGBT1 to rise. When V_{GE} exceeds the sum of the reverse bias voltage $-V_{GE}$ of IGBT1 and the threshold voltage, there is a possibility that the IGBT cause false turn-on. If IGBT1 cause false turn-on, IGBT1 and 2 turn on simultaneously, leading to a short-circuit condition.

To prevent false turn-on, methods include (a) increasing the reverse bias voltage $-V_{GE}$, (b) increasing R_g to reduce dVCE/dt. Additionally, as shown in Figure 3.7, (c) adding gate-emitter capacitance and (d) shorting the gate-emitter during the off state are also possible methods. However, there are side effects such as (a) increased surge voltage during off state, (b) increased turn-on losses, (c) increased gate drive losses, and (d) increased complexity of the gate circuit.

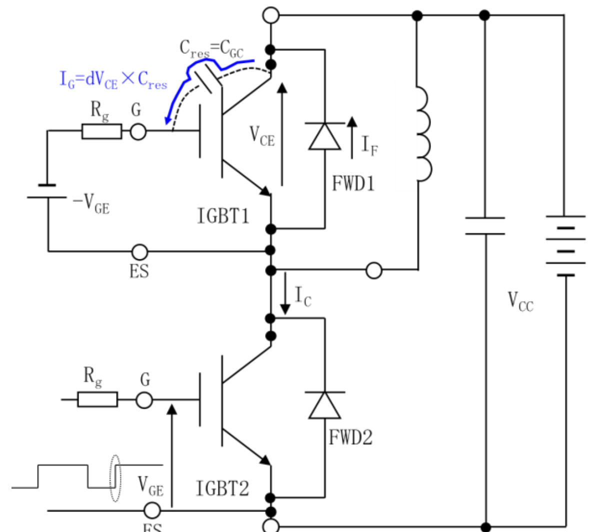
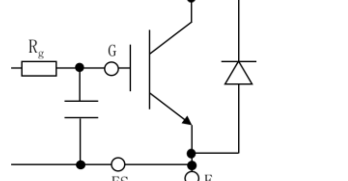
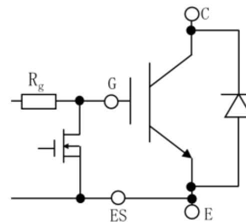


Figure3.6 The principle of false turn-on caused by V_{CE}/dt during recovery



(c) Insert capacitance between the G-E.



(d) Short G-E during the off state.

Figure3.7 False turn-on prevention methods

3-3-5. Gate drive power

The IGBT has a MOS gate structure and turns on and off by charging and discharging the gate capacitance. The peak value of the gate current I_{Gp} is determined by the following :

$$I_{Gp} = \frac{|+VGE|+|-VGE|}{R_g+rg} \quad \text{---(11)}$$

$+V_{GE}$: Gate forward bias

$-V_{GE}$: Gate reverse bias

R_g : Gate resistance of the drive circuit

r_g : Internal gate resistance of the IGBT module

Using the gate charge characteristic (V_{GE}-Qg) shown in Figure 3.8, it is possible to calculate the average gate current required to drive the IGBT and the gate drive power.

$$I_G=fc\times(|+Q_g|+|-Q_g|) \quad \text{---(12)}$$

fc: Carrier frequency

$+Q_g$: The amount of charge from 0V to $+V_{GE}$

$-Q_g$: The amount of charge from $-V_{GE}$ to 0V

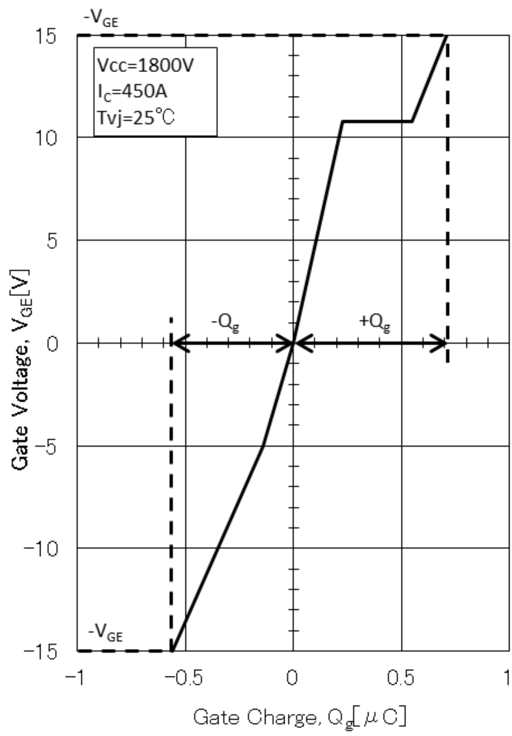


Figure3.8 Gate Charge Characteristics (V_{GE}-Qg): Typical

The gate drive power (P_d) is :

$$P_{d(on)}=P_{d(off)}=fc\times\{1/2\times(|Q_g|+|-Q_g|)\times(|+V_G|+|-V_G|)\} \quad \text{---(13)}$$

then,

$$P_d=fc\times(|Q_g|+|-Q_g|)\times(|+V_G|+|-V_G|)\} \quad \text{---(14)}$$

Please design the drive circuit to supply the drive current and drive power as described above. Additionally, select the power rating a gate resistance (Rg) that can adequately tolerate the losses calculated using Eq.(14).

3-3-6. Deadtime

The dead time is explained, including the basic concept of IGBT device operation. When the upper and lower arms turn on simultaneously, it results in an arm short circuit, causing overcurrent to flow through the device. Please set the dead time and overcurrent protection accordingly. The relationship between the dead time in logic and the dead time in the IGBT device is described below.

(1) Main Circuit Configuration Example

Figure 3.9 shows an example of the circuit configuration of a voltage-source inverter (single-phase). This example includes upper and lower arms between the P-N terminals of the DC voltage Eo. It assumes a mode where the IGBTs in the upper and lower arms alternately turn on and off. To prevent short circuits due to simultaneous turn-on (conduction), a dead time is set in the control signals for the off period of the upper and lower IGBTs. This period is also sometimes referred to as the non-overlap period.

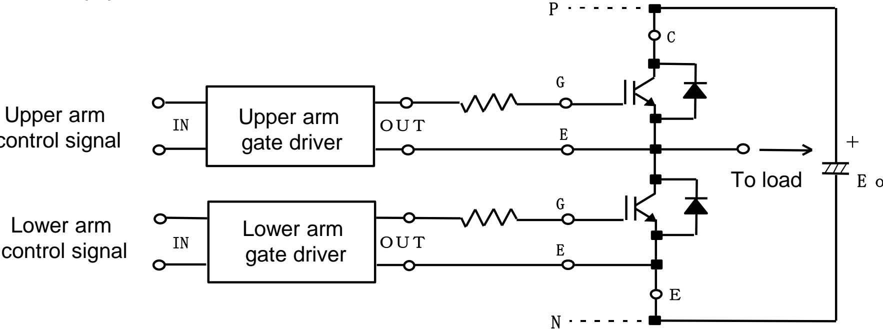


Figure3.9 An example of the main circuit configuration

(2) The dead time in the logic circuit and the dead time at the IGBT output terminals (C, E)

Figure 3.10 shows the phase relationship between the control signal, driver output voltage, and IGBT collector(C)-emitter(E) voltage. The dead time in the logic circuit (referred to as TD) is transformed into TD' due to the delay in the driver output voltage (t1, t3 in Figure 3.10) and the switching delay of the IGBT device (t2, t4 in Figure 3.10), resulting in a time difference.

Where t1～t4 are as follows,

t1 : The delay time between the on signal and the on-drive voltage output

t2 : The delay time between the on-drive voltage and the IGBT turn-on output

t3 : The delay time between the off control signal and the off-drive voltage output

t4 : The delay time between the off-drive voltage and the IGBT turn-off output

(It is assumed that there are no differences between the upper and lower arms for each of these delays)

The relationship between the dead time set in the theoretical (TD) and the dead time at the IGBT's CE terminal (TD') is given by the following

$$TD' = TD - (t3 + t4) + (t1 + t2) \quad \text{---(15)}$$

The dead time (TD) in the logic circuit changes based on the magnitude of the delay times t1 to t4, resulting in the actual dead time (TD'). Therefore, please consider and verify the delays in the driver system (t1, t3) and the delays in the IGBT devices (t2, t4).

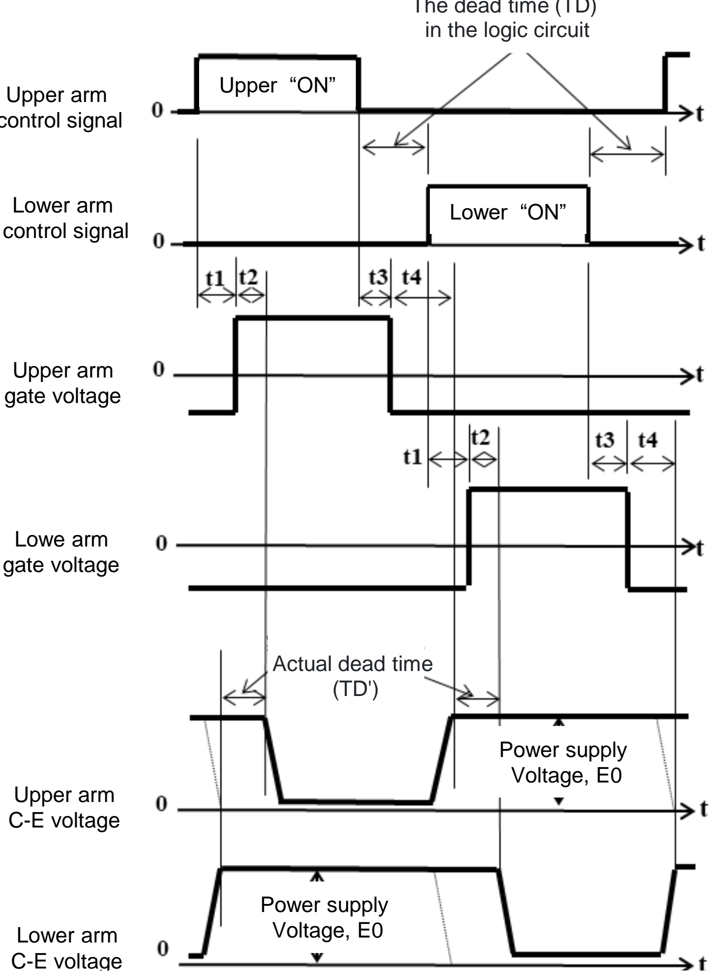


Figure3.10 The relationship between the control signal, driver voltage, and IGBT C-E voltage

(3) Verification of dead time

(a) Verification Circuit Configuration

Figure 3.11 shows a half-bridge circuit to explain the verification. the circuit operates on the assumption that the upper arm will turn on when the collector current of the lower arm is turn off, and signals are sent to the upper and lower driver circuits.

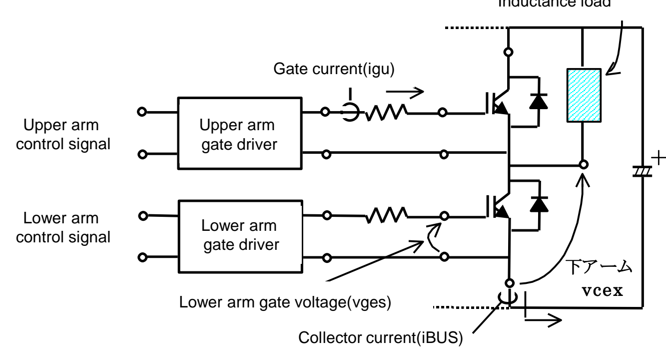


Figure3.11 Verification circuit (half-bridge)

(b) How to Observe Switching Waveforms

The non-overlap at the top and the bottom arm can be checked in various ways. Special care must be taken when observing voltage waveforms with different potential levels. Any floating-state voltage can be observed with an optical insulation cable or with a differential probe, but these methods require elaborate care delays and other factors.

(c)Confirmation of both arm operation

Figure 3.12 shows the waveforms during verification. The point at which the gate voltage of the lower arm transitions to reverse bias (Point B) and the peak point of the gate current of the upper arm (Point A) are used to determine whether there is overlap or non-overlap. If Point A precedes Point B, it can be inferred that a short circuit between the upper and lower arms has occurred (refer to Figure 3.12). When a short circuit between the upper and lower arms occurs, the collector current follows a pattern similar to the dashed line in Figure 3.12, leading to increased switching losses. In the gate voltage waveform at this time, an increase in the voltage value at Point B is observed.

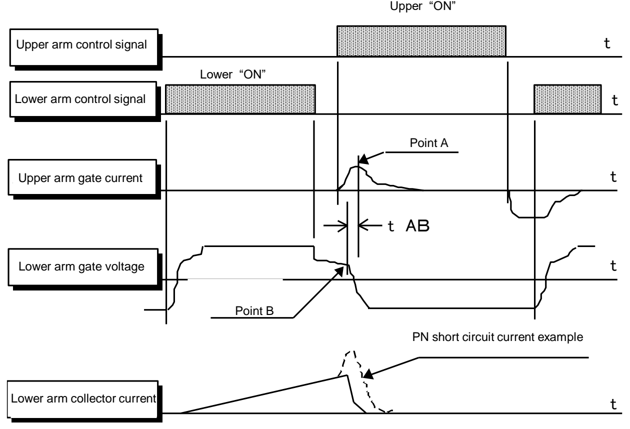


Figure3.12 Control signals and Upper/Lower arm gate waveforms

(d) Typical Verification

Figure 3.13 represents how a typical verification can be conducted in a circuit configuration as shown in Figure 3.11 and in waveform observations in Figure 3.12. This example has been observed with the control signal phase of the top arm changed. Figure 3.13 (1) shows the non-short-circuiting situation, while Figure 3.13 (2) reflects the short-circuited top and bottom arms condition.

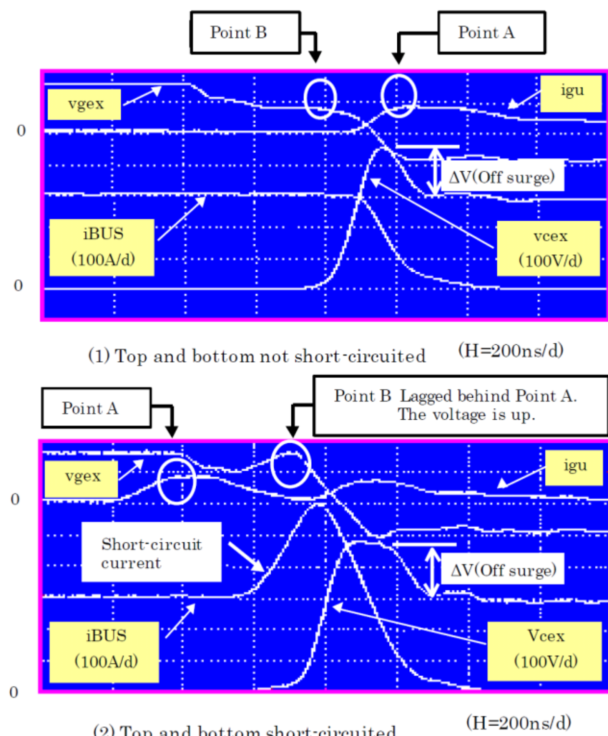


Figure3.13 Upper and Lower Arm Short-Circuited Waveform

1) Both top and bottom arms are not short-circuited （dead time is almost 0us）
2) Both top and bottom arms are short-circuited （300ns of short-circuit current flows through）

3-3-7. Cautions for the drive circuit power supply on the lower arm side

The drive circuit power supply on the lower arm side should be isolated for all three phases and should not share a common ground. The emitter on the lower arm side is electrically at the same potential under steady-state conditions. But during IGBT switching, the rate of change of the collector current (di/dt) can reach several thousand A/μs and this di/dt can induce a voltage of several tens of volts in the inductance of the wiring that constitutes the lower arm side main circuit, which is typically around several tens of nH. This induced voltage can adversely affect the switching of other phase IGBTs, such as by increasing the delay time.

Additionally, if the drive circuit power supply on the lower arm side is common, the voltage induced in the main wiring can appear as noise between the gate and emitter of the lower arm side IGBT of other phases through the common drive circuit power supply or common wiring. This can lead to malfunction or unstable switching conditions.

3-3-8. Wiring between the gate drive circuit and the IGBT terminals

(1) In order to minimize the distance between the gate drive circuit and the IGBT, directly connect the printed circuit board with the gate and emitter sense terminals.

(2) Keep the gate wiring and the P, N, and output terminals of the IGBT as far apart as possible. Therefore, do not cover the printed circuit board wiring above the P, N, and output terminals.

(3) When using a multilayer board for the gate drive circuit, layout of the gate wiring should not be overlapped vertically with that of other phases in the vertical direction.

(4) IGBTs are voltage-driven devices, similar to MOSFETs, and the impedance between the gate and emitter is very high. In such devices, if the driver is disconnected or the gate voltage bias is unstable due to factors such as the driver-side output impedance, applying a collector voltage causes a gate current to flow through the gate-collector capacitance (C_{GC}), thereby turning on the IGBT, as shown in Figure 3.14. Therefore, when powering up, first activate the gate drive power circuit to establish the gate voltage before applying the high-voltage power supply.

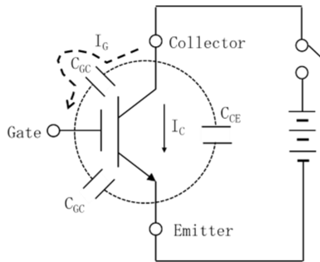


Figure3.14 When collector voltage is applied even though the gate is open

3-4. Dynamic avalanche

IGBT turn-off causes an increase in V_{CE}, but beyond a certain voltage, it is suppressed and does not rise further (refer to Figure 3.15). This phenomenon is known as dynamic avalanche. In simple terms, during turn-off, the channel of the MOSFET part closes, and the current begins to decrease. However, as the carriers remaining in the device disappear, they collide and ionize silicon atoms within the device due to the carriers passing through the high electric field inside the device, generating electron-hole pairs. These generated electrons and holes further collide with other silicon atoms, creating electron-hole pairs. This is the dynamic avalanche. When dynamic avalanche occurs, the current decay becomes small, and the V_{CE} overshoot voltage is suppressed. The voltage at which dynamic avalanche occurs varies depending on the current. An example is shown in Figure 3.16. When a dynamic avalanche occurs, it does not necessarily destroy the IGBT immediately, but rather the turn-off loss will be increased, and eventually the IGBT will be destroyed by latch-up. Therefore, during turn-off, please use within the range shown in Figure 3.16. Additionally, note that this range varies with temperature, and particularly at low temperatures, the range becomes narrower. Furthermore, If there are individual conditions for dynamic avalanche described in the specifications, please follow them.

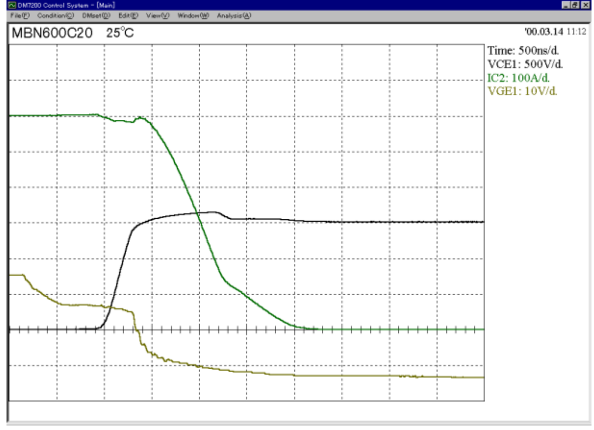


Figure 3.15 Example of waveforms during turn-off

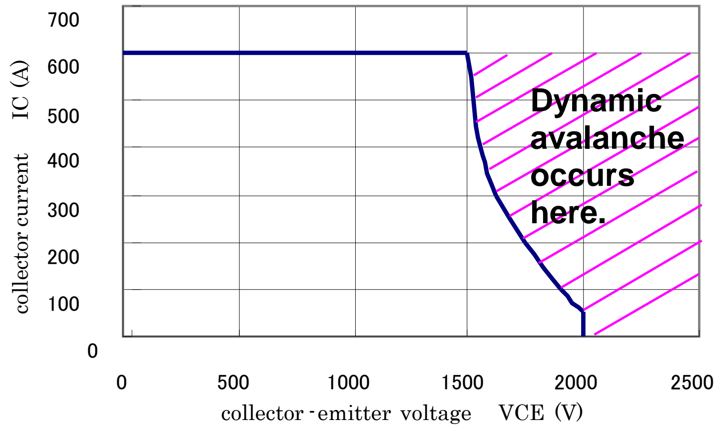


Figure 3.16 Example of regions where dynamic avalanche may occur.

3-5. Paralleling

3-5-1. Saturation Voltage Range [ΔVCE(sat)] Classify and Current Unbalanced Rate

When using high-voltage IGBTs in parallel connection, we as an option pair those with similar VCE(sat), however this pairing condition does not guarantee the parallel connections. Current imbalances occur because of unbalanced wiring inductance due to the physical structure of the equipment as well as the gate drive circuit and drive conditions, please use the product only after evaluating in advance. For more detailed information, we will decide through discussions with customer.

The definition of the current imbalance rate *α* during parallel connection is as follows:

$$\alpha = \left(\frac{I_{C'}}{(\mathrm{Itotal} \div 2)} - 1\right) \times 100(\%) \quad \text{---(16)}$$

Where I_C' : The current value of one element

I_{total} : Total current with two parallel connections

This definition is generally performed at the rated current value, but in the case of the same module, the imbalance rate α can vary significantly depending on the total current value, so please be cautious (α tends to increase at low currents). Additionally, in series connection, voltage sharing may not be uniform, and there is a possibility of overvoltage exceeding the voltage withstand capability of the elements. Therefore, in addition to static characteristics such as $V_{CE(sat)}$, it is necessary to consider dynamic characteristics such as td(on) and td(off), and to implement circuits to balance the voltage between the elements in series connection, such as voltage divider resistors and snubber circuits.

3-5-2. Parallel Connections and Current Derating

Although there is no limitation to the number of IGBT modules that can be connected in parallel, the negative effect reflected in an increase in the line inductance for power supply connections, e.g., surge voltage, etc. must always be taken account. For High Voltage IGBT, up to 4 parallel connections are realistic. Assuming worst-case condition that current is concentrated in one IGBT module, the current derating(R) is expressed by Eq.(17).

$$R = \frac{1 + (n-1) \times (1 - \frac{\alpha}{100}) \div (1 + \frac{\alpha}{100})}{n} \times 100(\%) \quad \text{---(17)}$$

Definitions:

n	Number of parallel connection
α	Current unbalanced rate

Ex. : 600A rated modules in 4 parallel with α set at 15%, the current reduction rate R would be 80.4%. Therefore, the total current in this case would be as follows:

600 A×4 parallel×0.804＝1,929 A

3-5-3. Considerations for parallel connections

(1) The basic considerations to be mindful of during parallel connections are as follows:

(a) Combining modules with small differences in $V_{CE(sat)}$ to minimize steady-state current imbalance.

(b) Minimizing wiring imbalances in the parallel layout of modules to reduce transient current imbalances during turn-on and turn-off.

(c) Ensuring symmetrical cooling conditions for parallel-connected modules to minimize temperature imbalances between modules.

Figure 3.17 illustrates an example of the implementation of modules and bus bars when two nHPD² packages are paralleled in a three-phase configuration. In this example, considerations are given to reducing the inductance of the DC and AC connection bus bars and ensuring symmetry.

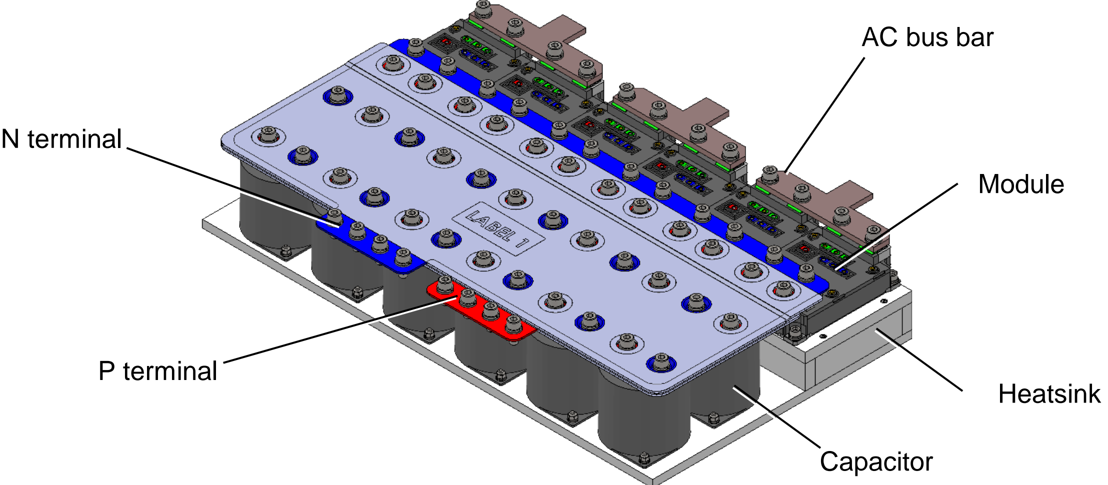


Figure 3.17 An implementation example of a three-phase inverter with two nHPD² packages connected in parallel.

(2) The number of drivers for one arm

When driving parallel-connected modules, the driver, which includes some signal processing circuits (such as optocouplers, amplifiers, and overcurrent protection circuits), should be configured with a single driver regardless of the number of parallel modules. This is to avoid negative effects on parallel operation due to variations in output delay times between drivers.

(3) The method of connecting gate resistors in parallel connection

Figure 3.18 shows a recommended arrangement to connect the gate resistor to the parallel circuit to minimize gate voltage variation due to mutual interference among the respective modules. In addition, attention needs to be paid to the following points :

(a) Make use of twisted pair cable for the driver output line to minimize line impedance.

(b) Have the same impedance (Lgst) in each loop (A and B) and minimize its value as much as possible.

Note: The objective of the recommendation described under items (a) and (b) is to avoid giving adverse effect due to inductance created when the main circuit is switched ON or OFF.

(c) Recognize the fact that the gate voltage variation stated above occurs when the main circuit is either turned ON or OFF. To avoid the variation, maintain the relationship between the gate resistor (RG) and loop inductance (Lgst) which can satisfy Eq.(18).

$$2 \times R_G > 2\sqrt{\frac{Lgst \times 2}{Cies/2}} \quad \text{---(18)}$$

Where Cies represents the gate input capacitance of the IGBT.

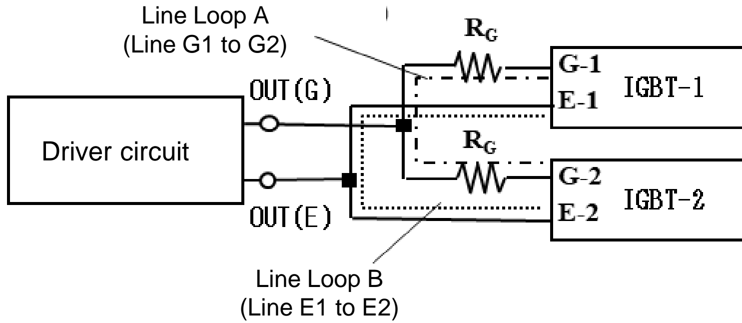


Figure3.18 Example of connecting parallel-connected modules and driver circuits

3-5-4. Necessity for Symmetry of Main Circuit Wiring

(1) Symmetry of Main Circuit Wiring

For IGBT modules to be connected in parallel, it is essential to equalize the wiring on the collector and the wiring on the emitter with each other to keep inductance values in balance. Figure 3.19 represents an example of parallel wiring of two modules and shows a schematic diagram of a parallel circuit including main circuit wiring inductance circuits. For the collector, wiring inductance circuit LCA and LCB are shown, and for the emitter, wiring inductance circuits LEA and LEB.

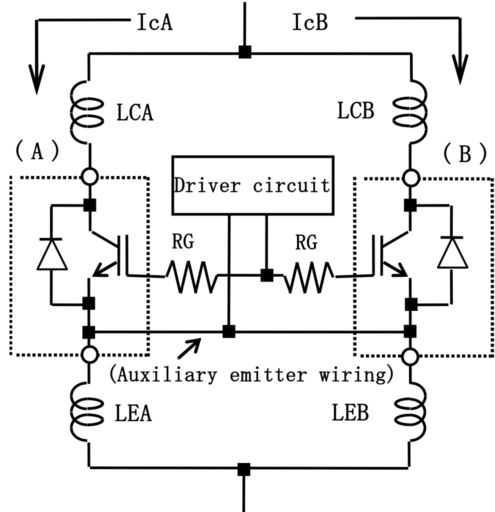


Figure 3.19 Wiring to Equalize Main Wiring Inductance Values

Wiring method to equalize LCA and LCB, LEA and LEB is required.

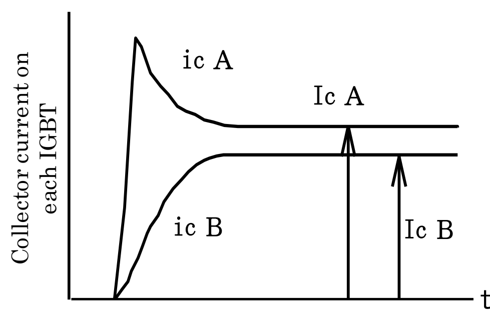
When the IGBT (A) and (B) are turning ON, the current generated on each individual collator depends on the variations of the inductance circuits rather than on each element's characteristics. Because the current balance depends principally on the inductance ratio, it is important to keep symmetry in wiring by matching the inductance values. For example, referring Figure 3.19, if wiring inductance of A and B sides are unbalanced (that is, LCA+LEA < LCB+LEB) and the VCE(sat) value of IGBT(A) is smaller, then the current sharing is depicted in Figure 3.13 will result. In particular, if emitter lines LEA and LEB are unbalanced, the IGBT gate voltage will be adversely influenced, causing an unbalanced current.

(2) Unbalanced Current Period caused by Wiring

Figure 3.20 shows that once a current imbalance occurs when turning ON an IGBT, it will be equalized during the steady-state condition after activating the IGBT, finally settling down to values IcA and IcB as determined by VCE(sat).

The time required for the unbalanced current to be equalized can be calculated as the attenuation over the L-R circuit caused by the inductance within the closed-loop forming a parallel circuit and the operating resistance of the IGBT element. The operating resistance "ron" can be easily calculated from the output characteristics curve.

For example, for an MBN1200E33E module having a single arm, an "ron" of approximately 3.4 milliohms (when Tj＝25℃、1/2 rated current) will be present. IF the loop inductance is 100nH for a parallel configuration, (LCA+LCB+LEA+LEB), the equalization in unbalanced current occurs based on the time constant τ is approximated by Eq.(19)



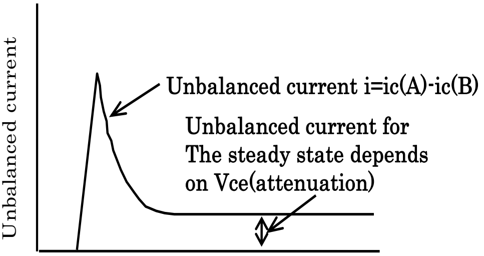


Figure 3.20 Equalization of Unbalanced Current

$$\tau = \frac{40\text{nH}}{7.7\text{m}\Omega \times 2} = 2.6\mu\text{s} \quad \text{---(19)}$$

If the stability in the current variation is assumed to be 3 times τ (that is, valuation is approximate, up to 95%), the current balance cannot be determined by VCE(sat) within 7.8μs after turning ON. This means if the carrier frequency is high or the active time is shorter, the current balance may be determined by the wiring (including the shape) for almost the whole period.

(3) Important considerations for gate wiring

When dealing with gate wiring in parallel connections, please pay attention to the following points:

(a) Ensure that each gate wiring and main circuit wiring are arranged orthogonally to prevent mutual induction and noise generation due to high potential differences. Additionally, maintain a sufficient distance between the gate wiring and the main circuit wiring.

(b) There is a high potential difference between the gate lines of the upper and lower arms. Ensure that there is adequate spacing between these wires.

(c) Keep the gate wiring of parallel elements as short as possible and make sure the wiring lengths are equal. This will help match the inductance values of each wire, thereby reducing variations in switching behavior due to differences in inductance.

3-5-5. Dynamic Avalanche and Parallel Connection

The dynamic avalanche voltage is lower than the rated voltage as shown in Figure 3.10, so when used in parallel and used beyond the area shown in Figure 3.16, more current flows toward the module which have lower dynamic avalanche voltage. An example is shown in Figure 3.21.
Figure 3.21 is a waveform for when there are no snubbers, but if there are snubber circuits, because the turn-off current is transferred to the snubber circuit, a decrease in collector current is faster than when there are no snubbers, so unbalanced current tends to occur in areas with high collector voltage. (See Figure 3.22)
In any case, when connected in parallel, be especially aware of unbalanced current and be sure to not use beyond the area shown in Figure 3.16.

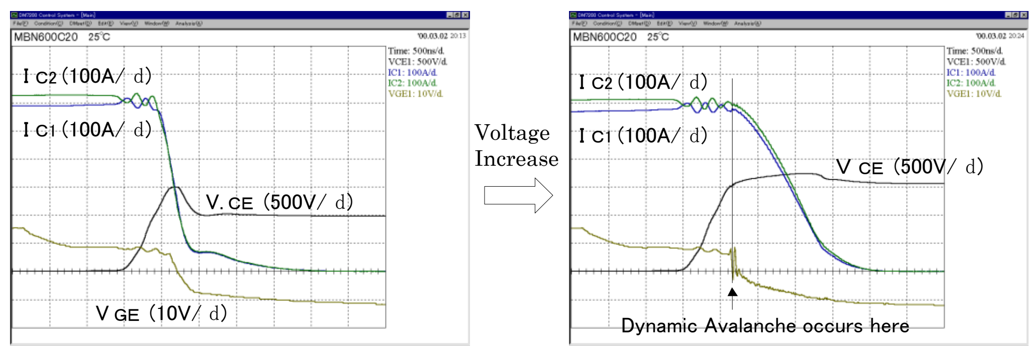


Figure3.21 Operation in parallel connection (without snubber).

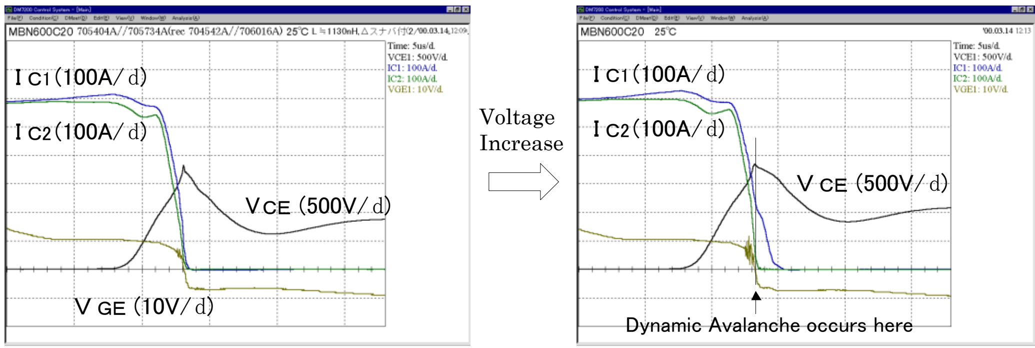
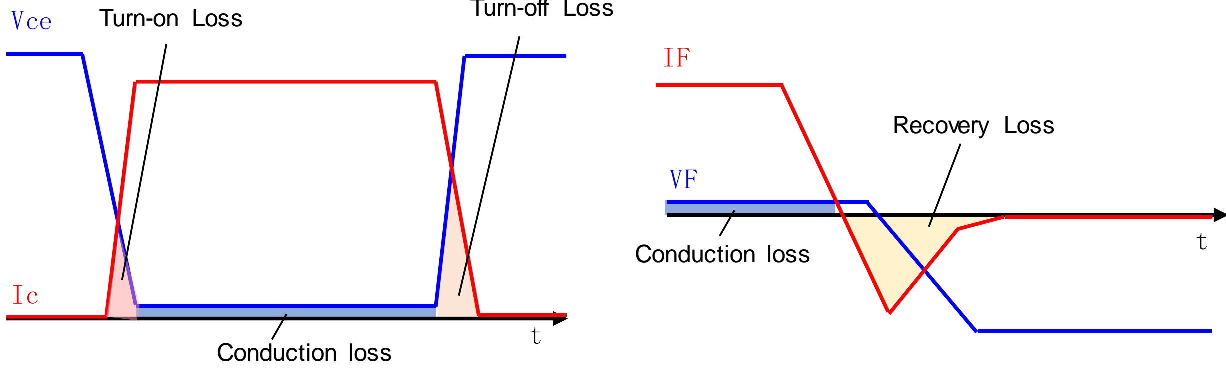


Figure3.22 Operation in parallel connection (with snubber).

3-6. Power loss of the IGBT module

3-6-1. Classification of IGBT module power loss

An IGBT module consists of IGBTs and diodes connected in parallel. The total loss of the IGBT module is the sum of the losses generated by both the IGBTs and the diodes. The generated losses include conduction losses during steady-state operation and switching losses that occur transiently during switching. Figure 3.23 illustrates the schematic switching waveforms and the generated losses for both the IGBT and the diode.



(a) The loss generated by the IGBT. (b) The loss generated by the diode.

Figure3.23 Schematic Switching Waveforms and Generated Losses of IGBT and Diode.

(Loss of module, P_{total})＝(Sum of arms)×{IGBT loss(P_{igbt})＋Diode loss(P_{diode})} ---(20)

P_{igbt}＝(Conduction loss, P_{on})＋(Turn-on loss, P_{ton})＋ (Turn-off loss, P_{toff}) ---(21)

P_{diode}＝ (Conduction loss, P_f)＋(Recovery loss, P_{rr}) ---(22)

3-6-2. Loss Calculation

This section introduces a simplified method for calculating losses when using IGBTs in a PWM-controlled inverter circuit. The following conditions are assumed for the calculation:

(a) PWM control of a three-phase, two-level inverter.

(b) The modulation method is sinusoidal pulse width modulation (SPWM) using triangular wave comparison.

(c) The output current is an ideal sinusoidal waveform.

Figure 3.24 shows the operational mode waveforms of the 2-level inverter based on the above assumptions.

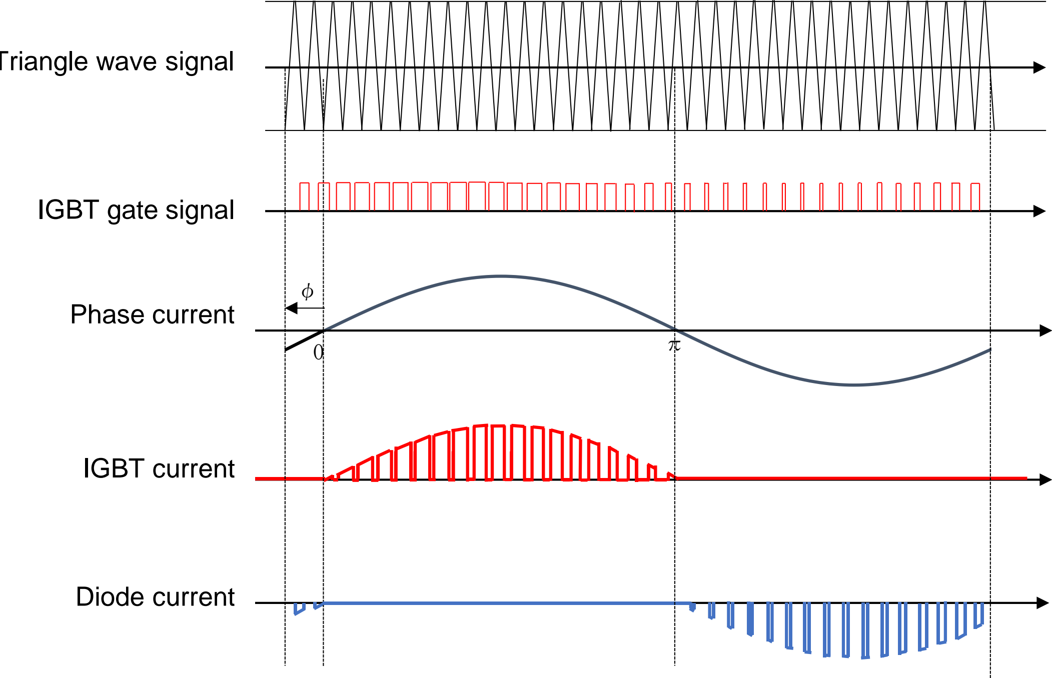


Figure3.24 Operational mode waveforms of the 2-Level Inverter.

(1) Conduction losses

The sinusoidal output current can be expressed by the following Eq.if the root mean square (RMS) value of the inverter's output phase current is I_o.

$$I_C = \sqrt{2} \times Io \times \sin\theta \quad \text{---(23)}$$

On duty waveform D(θ) can be expressed as (m : modulation, cosφ : Current lag power):

$$D = \frac{1+m\times\sin(\theta+\varphi)}{2} \quad \text{---(24)}$$

When the collector current I_C flows through the IGBT, a voltage $V_{CE(sat)}$ is generated between the collector and emitter. The relationship between $V_{CE(sat)}$ and I_C is provided in the datasheet. If the relationship between $V_{CE(sat)}$ and I_C is approximated linearly as shown in Figure 3.25(a), it can be expressed :

$$V_{CE(sat)} = a + I_C \times b \quad \text{---(25)}$$

Based on Eq.s (24) and (25), the IGBT losses per arm in the inverter circuit, when the modulation index (m = 1), can be expressed as follows:

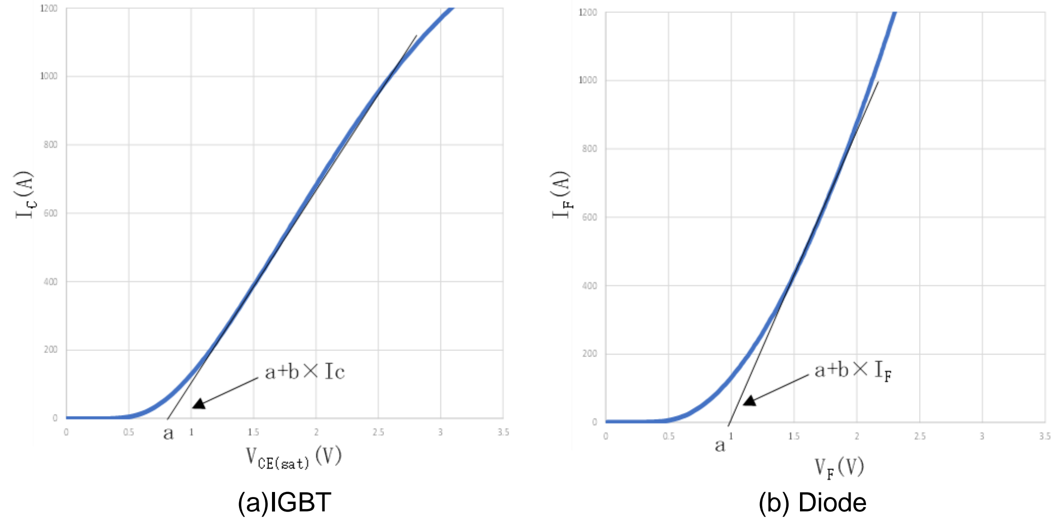
$$P_{on} = \frac{1}{2\pi}\int_0^{\pi} I_C \times V_{C\,(sat)} \times D \times d\theta$$
$$= \frac{\sqrt{2}Io}{2\pi} a + \frac{1}{4} bIo^2 + \frac{m}{24\pi} \cos\varphi \left(3\pi\sqrt{2}aIo + 16bIo^2\right) \quad \text{---(26)}$$

Where I_C : The collector current (instantaneous value) flowing through the IGBT, $V_{C(sat)}$: The saturation voltage (instantaneous value) of the IGBT.

Similarly, if the relationship between V_F and I_F for the diode is approximated linearly as shown in Figure 3.25(b), it can be expressed by the following Eq.(27):

$$V_F = a + I_F \times b \quad \text{---(27)}$$

$$Pf = \frac{1}{2\pi}\int_{\pi}^{2\pi} I_F \times V_F \times D \times d\theta$$
$$= \frac{\sqrt{2}Io}{2\pi} a + \frac{1}{4} bIo^2 - \frac{m}{24\pi} \cos\varphi \left(3\pi\sqrt{2}aIo + 16bIo^2\right) \quad \text{---(28)}$$



(a)IGBT (b) Diode

Figure3.25 Linear approximation of IGBT and Diode output characteristics.

(2) Switching losses

The method for calculating switching losses from the I_C dependency of Eon, Eoff, and Err as described in the datasheet is as follows. When the I_C dependency of E_{on} using a linear approximation, the following Eq.(29) can be used:

$$E_{ON}(I_C) = k_{on} \times I_C \quad \text{---(29)}$$

Then, P_{ton} can be expressed as:

$$\begin{aligned} P_{ton} &= \frac{1}{2\pi}\int_0^{\pi} E_{on}(I_C) \times fsw \times d\theta \\ &= \frac{1}{2\pi}\int_0^{\pi} k_{on} \times \sqrt{2} \times I_o \times \sin\theta \times fsw \times d\theta \\ &= \frac{\sqrt{2}}{\pi} \times k_{on} \times I_o \times fsw \quad \text{---(30)} \end{aligned}$$

Where fsw means carrier frequency.

The average of the output current I_{ave} is expressed by the following :

$$I_{ave} = \frac{2}{\pi} \times \sqrt{2} \times I_o \quad \text{---(31)}$$

If Eon at I_{ave} is E_{ton}, then Eq.(31) becomes

$$P_{ton} = Eton \times \frac{fsw}{2} \quad \text{---(32)}$$

Similarly

$$P_{toff} = Etoff \times \frac{fsw}{2} \quad \text{---(33)}$$

$$P_{rr} = Err \times \frac{fsw}{2} \quad \text{---(34)}$$

3-7. Thermal Resistance and Heat Dissipation Design

3-7-1. Thermal Resistance

The thermal resistance of the module is specified in the specifications for both the IGBT and diode devices, particularly the junction-to-case thermal resistance $R_{th(j-c)}$.

3-7-2. Definition of Temperature Measurement Locations

The definitions for the measurement locations of the case temperature and the heat sink temperature are shown in Figure 3.26. The junction-to-case thermal resistance $R_{th(j-c)}$, and the case-to-heat sink contact thermal resistance $R_{th(c-f)}$ are specified based on these definitions.

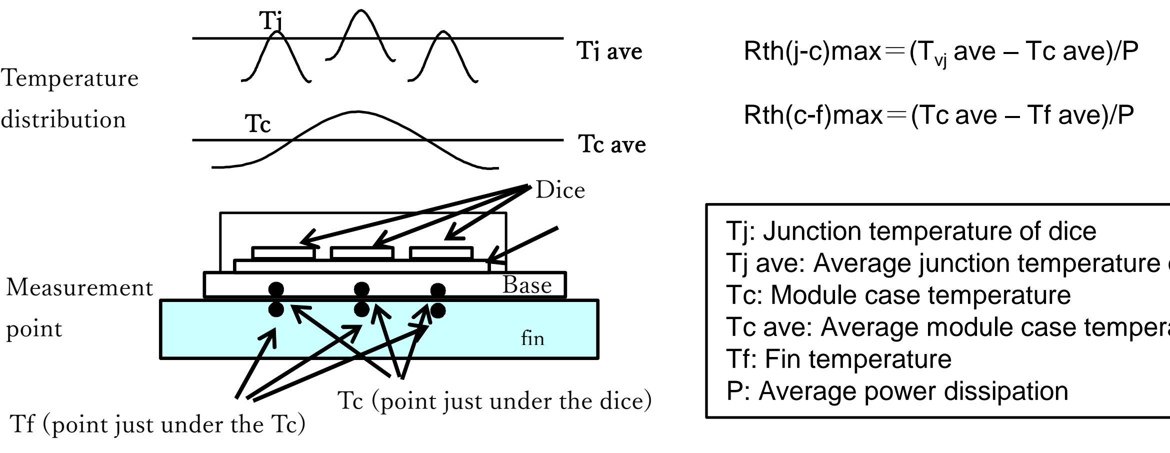


Figure3.26 Locations of temperature measurement.

3-7-3. Heat Dissipation Design

The basic concept for selecting heat sinks for steady-state and transient conditions are the following.

(1) Steady state

The thermal equivalent circuit for the steady-state condition is shown in Figure 3.27. Using the thermal equivalent circuit in Figure 3.27, the junction temperature of the IGBT, T_{vj}(IGBT), can be determined by the following Eq.(35):

$$T_{vj}(IGBT) = P(IGBT) \times Rth(j\text{-}c)(IGBT) + \{P(IGBT)+P(Diode)\} \times Rth(c\text{-}f) + \{P(IGBT)+P(Diode)\} \times Rth(f\text{-}a) + Ta \quad \text{---(35)}$$

The difference between the junction temperature and the ambient temperature, denoted as ΔT_{vj}(IGBT) is given by the following:

$$\Delta T_{vj} = P(IGBT) \times Rth(j\text{-}c)(IGBT) + \{P(IGBT)+P(Diode)\} \times Rth(c\text{-}f) + \{P(IGBT)+P(Diode)\} \times Rth(f\text{-}a) \quad \text{---(36)}$$

Here, the measurement points for the case temperature Tc and the heat sink temperature Tfare defined according to the temperature measurement locations in Figure 3.26.

Additionally, to determine the junction temperature of the diode, the temperature rise between the junction and the case can be calculated as P(Diode)×Rth(j-c)(Diode) , and the same approach as for IGBT can be applied.

Please note that if the case temperature measurement location differs, the thermal resistance will also differ from the catalog values, so caution is required.

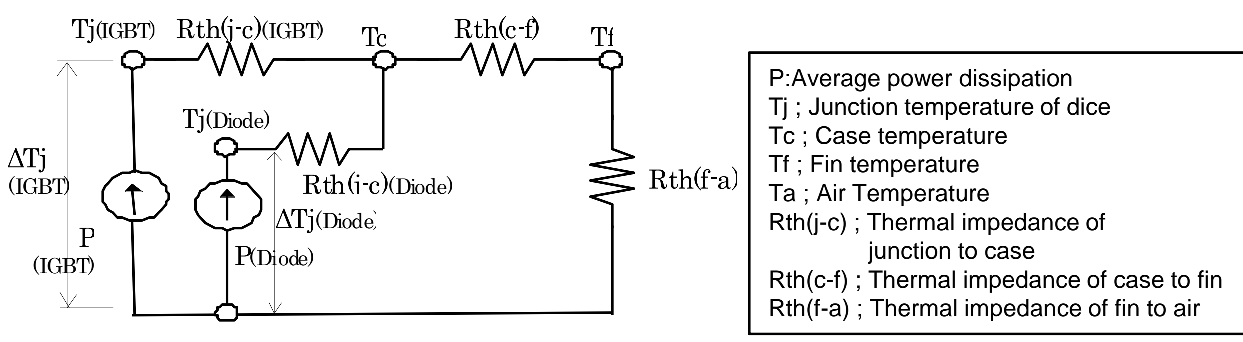


Figure3.27 Thermal equivalent circuit.

(2) Transient state

In general, it is sufficient to consider the average generated losses for the steady-state junction temperature T_{vj} based on the case temperature T_c. In reality, IGBTs repeat switching, generating pulsed losses. If the generated loss is considered to be a continuous square wave pulse with a constant period and a constant peak value, the peak value of the junction temperature, Tvjp, can be found by Eq.(37) using the transient thermal resistance characteristic curve shown in Figure 3.29.

$$T_{vjp}=P1\times\{Rth(Steady)\times t1/t2+(1-t1/t2)\times Rth(t1+t2)-Rth(t2)+Rth(t1)\}+Tc \quad \text{---(37)}$$

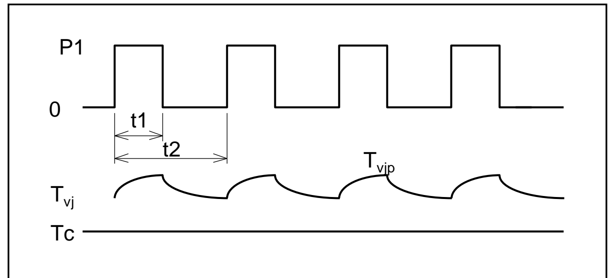


Figure3.28　Temperature ripple

Figure3.29 Transient thermal resistance

Figure 3.30 shows the temperature ripple during inverter operation. The junction temperature oscillates with the same cycle as the output frequency. It also oscillates with the same cycle as the carrier frequency. Taking these things into consideration, T_{vj} must never exceed T_{vjmax} even for a moment.

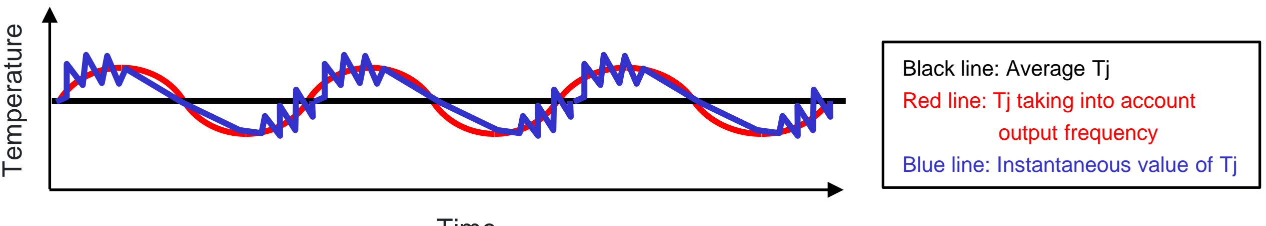


Figure3.30 Temperature ripple during inverter operation.

3-7-4. Notes on temperature ripple and temperature variation

(1) Points to note when there is temperature ripple:

(a) Consider factors such as those in the previous section and make sure that the temperature ripple peak value of the junction temperature does not exceed the rated value (T_{jmax}) when selecting the fin.

(b) Stress applied to structural parts inside the module increases with the size of the temperature ripple, and the risk of reducing the life time of the module increases with the number of cycles. In particular, carefully consider applications where high temperature ripples occur, and moreover, where there are a large number of cycles.

(c) In addition, note that if the generated loss changes with respect to time, case temperature (Tc) may also change according to the incurred loss due to the presence of case to fin contact thermal resistance.

(2) Module Lifetime Curve under Power Cycle Operating

There is a power cycle capability in the life category of the mode where junction temperature (Tj) of the device changes and the cooling system and module case temperature (Tc) do not change much.

This shows the relationship between the change swing (ΔTj) of the module temperature change and the repeat cycle number (N). The power cycle capability mainly represents a degradation mode in which the bonding area of the wire is stressed, causing $V_{CE(sat)}$ to increase. Our testing method involves passing the rated current through DUT(Device Under Test) for several seconds, followed by a period of being off for several seconds to induce a change in the junction temperature, defining this as one cycle.

In practical use, the presence of thermal contact resistance between the module's case and the heat sink cannot be ignored, and the case temperature may also change. Therefore, ΔT_{vj} should be evaluated between the junction and the heat sink.

3-7-5. Power cycle lifetime in actual devices

When using power modules for inverters to control motors, the operating conditions of the power modules change complexly in accordance with the motor operation conditions such as starting, acceleration (traction), coasting, deceleration (regeneration), and stopping. The losses generated in the power modules due to these conditions cause the power modules to repeatedly heat up and cool down, resulting in complex fluctuations in the chip temperature T_{vj}. Because this temperature change induces thermal stress on the power modules, the lifetime of the power modules primarily determined by the power cycle lifetime due to T_{vj} swing during actual operation. To estimate the product lifetime of power modules in the field, it is necessary to obtain the operation patterns of the inverters in the field and determine the operating conditions of the power modules.

Figure 3.31 illustrates estimation method of power cycle lifetime. The operation pattern of the inverter includes the current, voltage, modulation factor, power factor, and switching frequency. Using these values and the I_C-V_{CE} characteristics, I_F-V_F characteristics, I_c-Eon/Eoff, and I_F-Err characteristics, the loss history of the IGBT and diode is calculated. From this loss history and transient thermal resistance, the junction temperature T_{vj} and case temperature T_c of the IGBT and diode are calculated. The temperature swing ΔT_{vj} and its cycle count are summarized from the T_{vj} history, and the power cycle lifetime is calculated. Generally, the T_{vj} of the IGBT and diode forms a complex and non-periodic waveform, so the rainflow-counting algorithm is used to convert the waveform of T_{vj} into multiple ΔT_{vj} and their cycle counts.

Figure 3.32(a) shows an example of a temperature history. In the rainflow-counting algorithm, ΔT_{vj} is classified into four components as shown in (b). Specifically, it is classified into a large $+\Delta T_{vj1}$ and a small $-\Delta T_{vj2}$ as shown in blue in (c), and a large $-\Delta T_{vj3}$ and a small $+\Delta T_{vj4}$ as shown in yellow in (d).

The power cycle capability is expressed by the following Eq.as a function of ΔT_{vj}, maximum temperature $T_{vj,max}$, and on state time t_{on}:

$$N = N_0\left(\Delta T_{vj}\right)^n \cdot t_{on}^m \cdot \exp\left(\frac{Q}{k_B\left(273+T_{vjmax}\right)}\right) \quad \text{---(38)}$$

Where n, m:constant values, Q : activation energy (eV), k_B : Boltzmann constant 8.6173×10^{-5}(eV/K)

Using Eq.(38), the damage factor D is calculated in Eq.(39), and then the actual power cycle lifetime N is calculated from the cycle count at which D=1 in Eq.(40).

$$D = \Sigma_{i=1}^{n}\left(\frac{1}{N_i}\right) = \Sigma_{i=1}^{n}\left(\frac{1}{N_0\left(\Delta T_{vj,i}\right)^n \cdot t_{ON,i}^m \cdot \exp\left(\frac{Q}{k_B\left(273+T_{vjmax,i}\right)}\right)}\right) \quad \text{---(39)}$$

$$N = \frac{1}{D} \quad \text{---(40)}$$

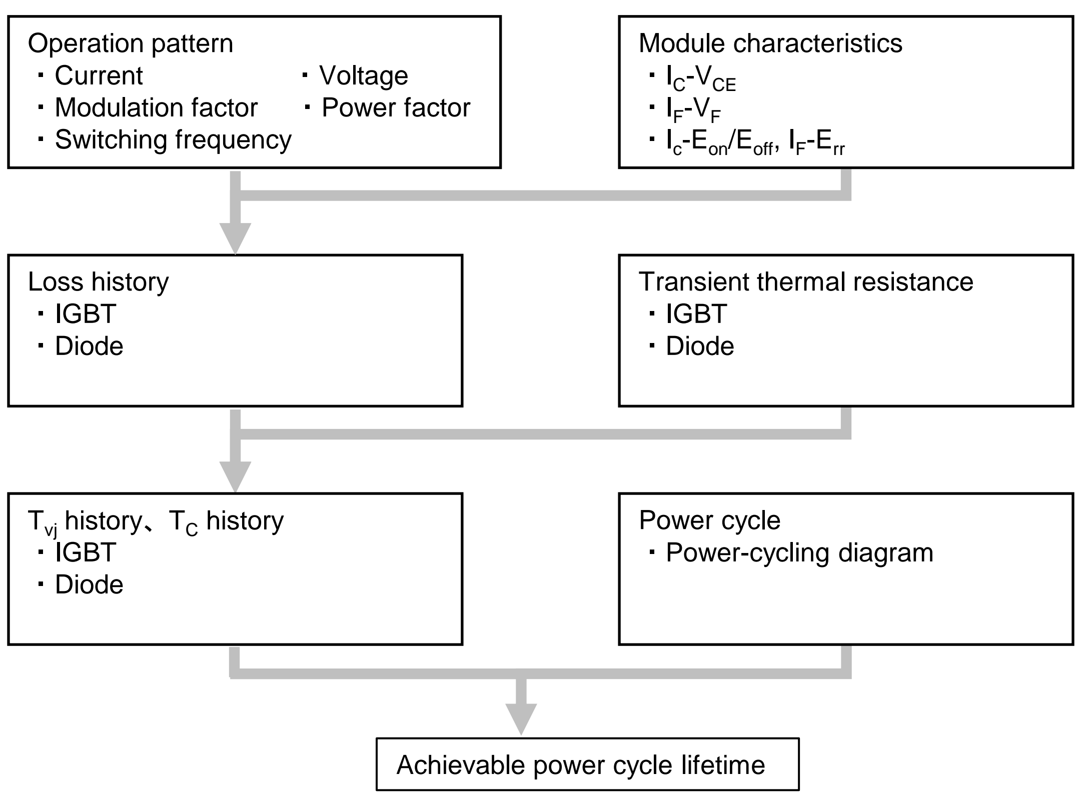


Figure 3.31 Estimation method of achievable power cycle lifetime

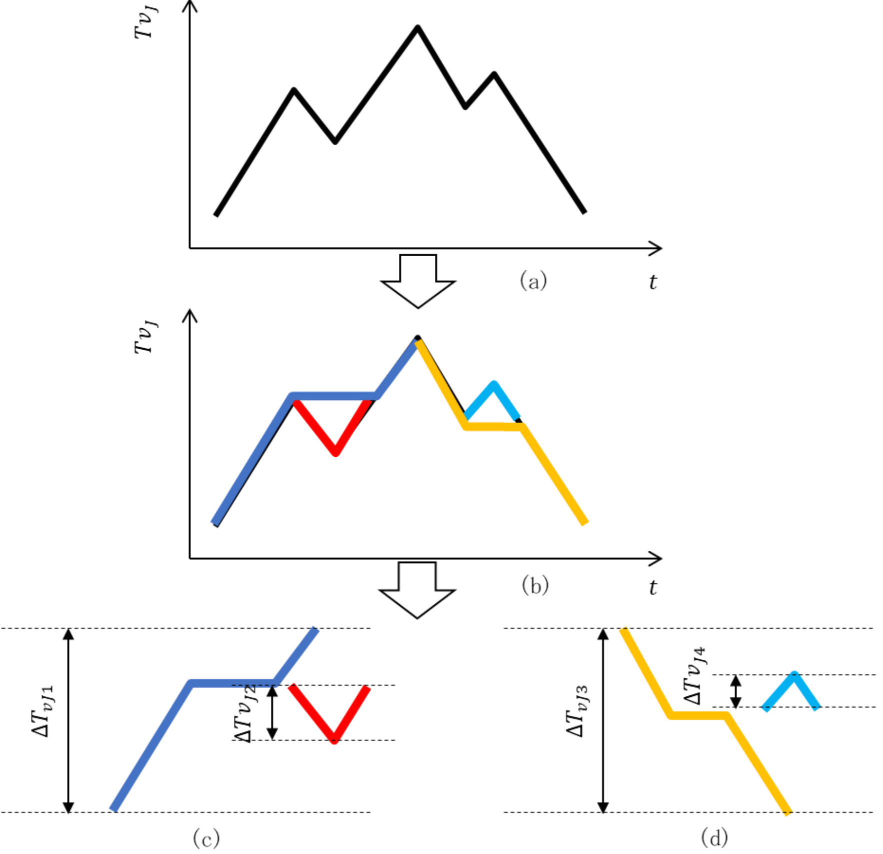


Figure 3.32 Rainflow-counting algorithm

3-7-6. Temperature Monitoring of Power Modules Using a Thermistor

In power modules which are equipped with NTC(Negative Thermal Coefficient) thermistors, it is possible to monitor the temperature of the operating power module. There is an exponential relationship between the resistance R of the NTC thermistor and the absolute temperature T_r of the thermistor, which can be approximated by the following Eq.(41).

$$R = R_0 \cdot \exp\left(B\left(\frac{1}{T_r} - \frac{1}{T_0}\right)\right) \quad \text{---(41)}$$

Where, B represents the constant value, which characterizes the temperature dependence of the resistance of the thermistor, and R_0 represents the resistance of the thermistor at the reference temperature T_0.

Using the relationship expressed by Eq.(41), temperature estimation is possible by measuring its resistance. However, since Eq.(41) involves approximation errors, a more accurate temperature measurement can be achieved by referring to the R-T characteristic curve of the thermistor, as shown in Figure 3.33.

It is important to note that the thermistor is mounted at a location separate from the IGBT chip or diode chip inside the power module, so the thermistor temperature T_r may differ from the junction temperature T_{vj}. The relationship between T_{vj} and T_r varies depending on the operating conditions of the power module. Therefore, T_{vj} can not be estimated by the thermistor. Under general operating conditions, the following relationships hold true among the thermistor temperature T_r, junction temperature T_{vj}, and case temperature T_C.

$$T_C < T_r < T_{vj} \quad \text{---(42)}$$

Under general operating conditions, $T_C \approx T_r$ under steady-state conditions. Therefore, it is possible to use the thermistor to detect long-term T_C rise (about 1 minute) due to abnormalities in heat dissipation grease, heat sinks, or cooling water temperature.

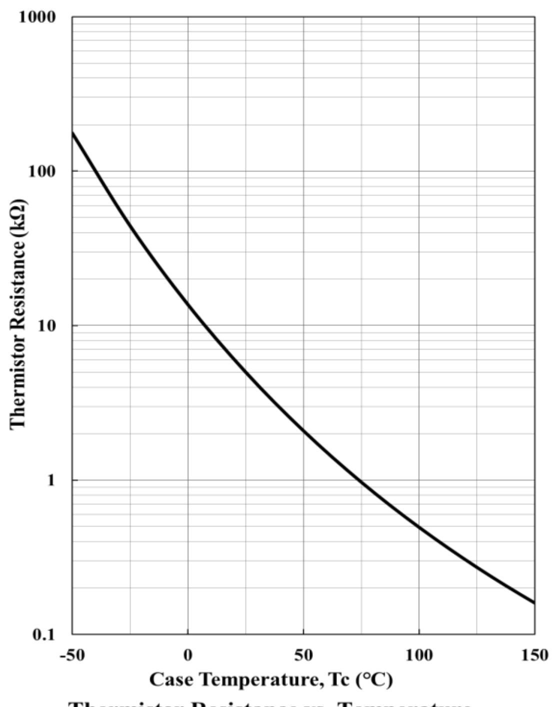


Figure 3.33 Relationship between resistance(R) and temperature(T) of NTC thermistor：typical

3-7-7. Thermal interference between IGBT and diode

Because the IGBT chips and diode chips are placed close together in a power module, the temperature of the diode chips rises due to the losses of the IGBT. Similarly, the temperature of the IGBT chips rises due to the losses of the diode. This phenomenon is known as thermal interference. Under actual operating conditions of the power module, both the IGBT and diode generate losses, so it is necessary to consider thermal interference to estimate the T_{vj} of both the IGBT and diode.

Figure 3.34 shows the results obtained from simulations of the T_{vj} of the IGBT and diode when both chips are simultaneously generating loss. The horizontal axis of the figure shows the ratio of the losses of the IGBT and diode, with the left end indicating 100% IGBT losses and 0% diode losses, and the right end indicating 0% IGBT losses and 100% diode losses. In each simulation, the total losses of the IGBT and diode are kept the same. From the figure, it can be observed that the T_{vj} of the IGBT or diode increases even when the other device is not generating heat

Figure 3.35 shows an example of a thermal equivalent circuit that represents the calculation results of Figure 3.34. By using a Y-shaped equivalent circuit, it is possible to represent the thermal interference between the IGBT and diode.

	Power dissipation ratio				
IGBT	100%	75%	50%	25%	0%
Diode	0%	25%	50%	75%	100%

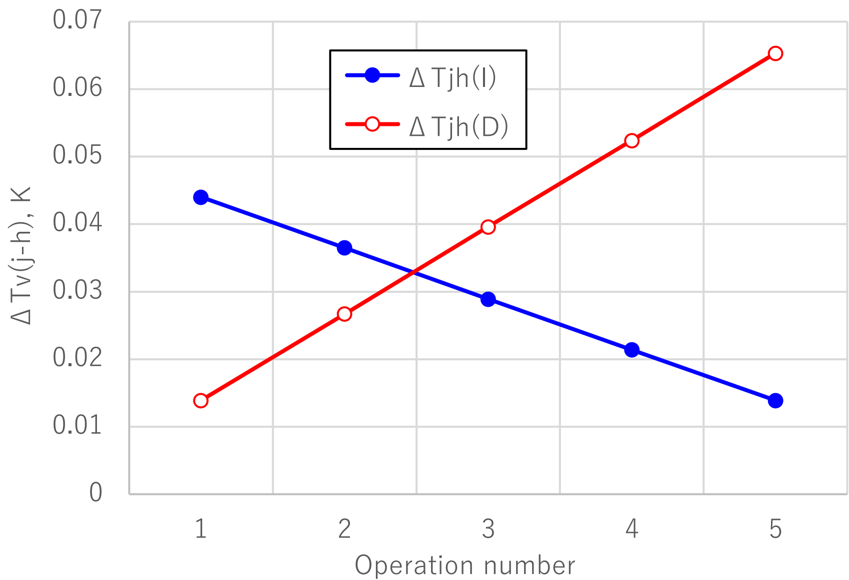


Figure 3.34 Relationship between IGBT and diode loss ratio and Tvj (Simulation)

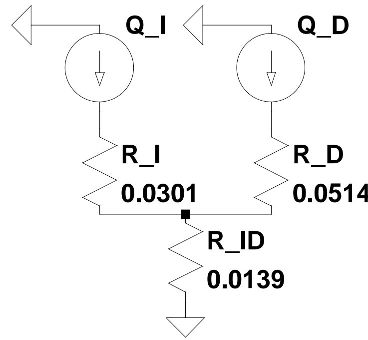


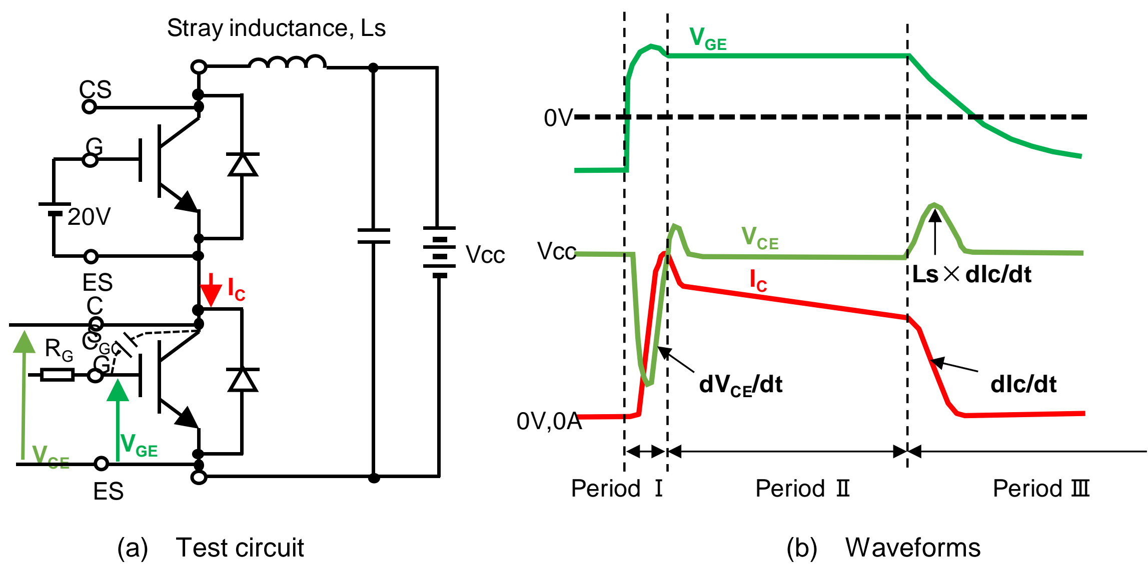
Figure 3.35 Example of a thermal equivalent circuit model expressing the thermal interference between an IGBT and a diode

3-8. Protection Circuit

3-8-1. Short Circuit / Overcurrent

(1) Arm Short Circuit

Figure 3.36 shows schematic waveforms of IGBT short circuit test. If the IGBTs on the upper and lower arms turn on at the same time, the collector current I_C of the IGBTs rapidly increase . When I_C reaches the saturation current of the IGBT, the collector voltage V_{CE} also rises rapidly to a high voltage level. If this condition continues, the IGBT will be destroyed by thermal runaway. Short-circuit withstand time is defined as the time during which an IGBT can turn-off without destruction. The delay time from a short circuit detection of the protection circuit to turn-off must be shorter than the short-circuit withstand time. The short-circuit withstand time depends on V_{CE}, V_{GE}, and T_{vj}, and generally decreases as the power supply voltage V_{CC} and V_{GE} increase, and as T_{vj} increases.



(a) Test circuit (b) Waveforms

Figure 3.36 Schematic waveforms of IGBT short circuit test

The waveform can be divided into three periods below.

Period I : The IGBT turns on, and current begins to flow. The V_{CE} decreases due to the stray inductance Ls and the collector current change rate dI_C/dt. As dI_C/dt decreases, V_{CE} increases and a dV_{CE}/dt occurs. This dV_{CE}/dt causes the gate current which flow from the collector to the gate through the gate-collector capacitance $C_{gc.}$ This gate current cause increase of gate voltage above the gate supply voltage. This gate voltage increase the collector current I_C and cause the peak of the Ic. Note that the gate voltage at this time must not exceed the absolute maximum gate voltage. Additionally, if the peak Ic is too high, latch-up destruction may occur. Since dV_{CE}/dt is highly dependent on the turn-on gate resistance, careful attention should be paid when setting it.

Period II : Due to the self-heating of the IGBT, the junction temperature T_{vj} increases over time and T_{vj} rise cause I_C decrease.

Period III : The gate turns off, and a voltage spike of Ls × dI_C/dt occurs. At this time, if the IGBT is turned off with the usual turn-off gate resistance, the Short Circuit Safe Operation Area (SCSOA) may be exceeded by the large saturation current and the voltage spike. Therefore, it is recommended to set the turn-off gate resistance during short-circuit detection to a higher value than the usual turn-off resistance.

(2) Output Short Circuit and Ground Fault

Figure 3.37 shows the current paths for output short circuit and ground fault. An output short circuit occurs when the motor fails or when the control or gate circuit is stuck in a certain phase.

Figure 3.38 shows the circuit and waveform of a simulated output short circuit test. In an output short circuit, in addition to the stray inductance L_s between the smoothing capacitor and the module, the short circuit path includes the motor inductance and the inductance L_C of the wiring cables between the inverter and the motor. The inductance of the short circuit path is calculated as follows:

$L_{sh} = L_S + L_C$ ---(43)

The current change rate di/dt can be expressed by the following Eq.(44), considering the power supply voltage as V_{CC} :

$di/dt = V_{CC}/L_{sh}$ (A/sec) ---(44)

and ts(sec) is the time from the start of the short circuit, the collector current I_C can be expressed by the following Eq.:

$I_C = di/dt \times ts$(A) ---(45)

When the collector current I_C reaches the saturation current, the collector voltage V_{CE} increases. Similar to the case of an arm short circuit, this results in significant heat generation because the saturation current of the IGBT flows with a high voltage V_{CC}.

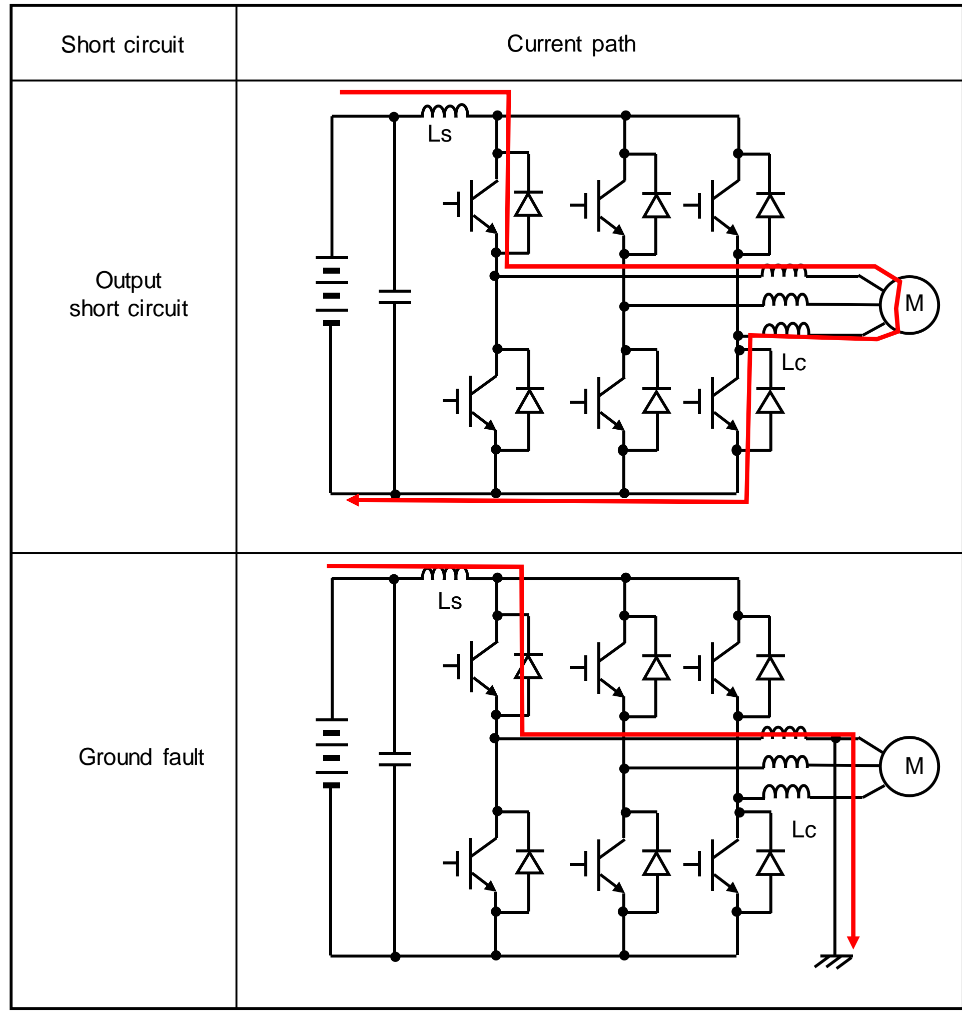
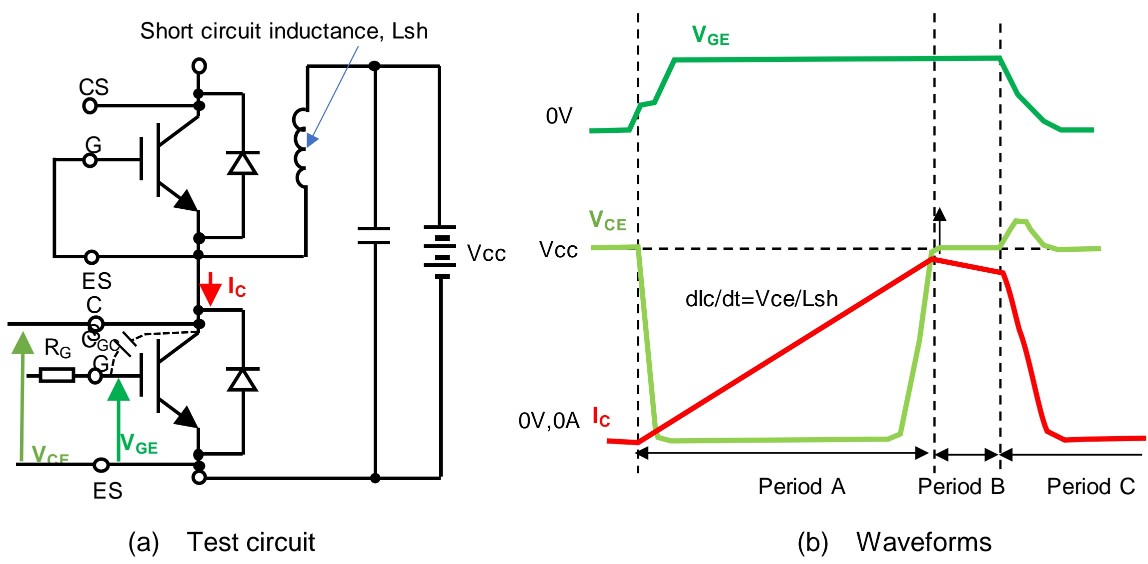


Figure 3.37 Output short circuit and ground fault current paths

If the cable between the inverter and the motor or the motor itself experiences a ground fault, the waveform will be similar to that shown in Figure 3.38.



(a) Test circuit (b) Waveforms

Figure 3.38 Output short circuit simulated test circuit and waveforms

3-8-2. Overvoltage

(1) Causes of overvoltage

During IGBT turn-off or diode recovery, the current change rate di/dt causes a surge voltage due to the wiring inductance L_s between the IGBT module and the smoothing capacitor. The peak voltage V_{cp} of the turn-off surge voltage can be expressed by the following Eq., considering the DC voltage as V_{CC}:

$$V_{cp}=V_{CC}+ di/dt \times Ls \quad ---(46)$$

Under the maximum DC voltage conditions in the system, please ensure that the transient characteristics (locus) of voltage and current are within the RBSOA and RRSOA.

(2) Suppress surge voltage

The following are methods to suppress surge voltage:

(a) Adjust the gate resistance and negative bias of the IGBT drive circuit to suppress di/dt. This will be explained in detail at section 3-3 "Gate Drive Circuit".

(b) Place the smoothing capacitor as close to the IGBT module as possible. Additionally, use capacitors with low stray inductance, such as film capacitors.

(c) To reduce stray inductance L_s, use thick and short busbars for wiring. It is also effective to use laminated busbars for parallel flat plate wiring (PN wiring).

(3) Example of surge voltage characteristics

Figure 3.39 shows an example of the collector current dependency of surge voltage during IGBT turn-off and diode recovery. The IGBT turn-off surge voltage V_{CEP} increases as the collector current I_C becomes larger. On the other hand, the diode recovery surge voltage V_{AKP} tends to be higher at lower current levels. As such, surge voltage varies depending on voltage and current conditions, drive conditions, drive (ambient) temperature, and circuit conditions. Therefore, ensure that the transient characteristics (locus) of voltage and current are within the RBSOA and RRSOA specified in the datasheet under all operating conditions expected for the system.

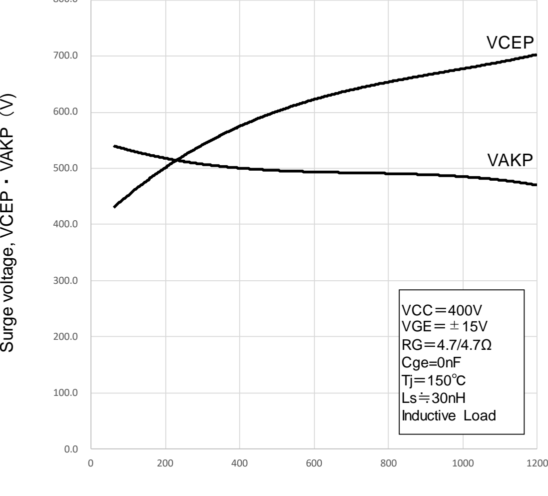


Figure3.39 Collector current dependency of surge voltage during IGBT turn-off and diode recovery.

4. Mounting Instructions

4-1. Module assembly onto the heat sink

4-1-1. Recommended Tightening Torque

Table 4.1 shows the recommended torque for preliminary and final tightening。

Table 4.1 Recommended torque values for mounting IGBT modules.

No	Screw	Rated Torque (N・m)	Recommended torque (N・m)	Temporary tightening torque (N・m)	Final tightening torque (N・m)
1	M6	6.0	5.5	1.5~2.0	4.9~5.9

4-1-2. Method for Applying Thermal Grease (Thermal Compound)

(1) Purpose

An appropriate thermal interface is an important for mounting a power module to a heatsink. Thermal grease is widely used as a thermal interface material to reduce thermal resistance between the power module and the heatsink. To achieve an effective thermal interface, it is necessary to use the grease correctly. Incorrect use of the grease can lead to overheating of the chip and potentially resulting in the destruction of the module.

(2) How to use thermal grease

We would like to introduce the method we have verified for mounting to a heatsink. The optimal mounting method varies depending on the shape of the heatsink. Therefore, this is presented as an example and does not guarantee the implementation state. Figure 4.1 shows the workflow of coating thermal grease, and Figure 4.2 shows an example of the stencil pattern used in the workflow.

The steps are as follows:

Step1：Set stencil mask

Remove any foreign objects from the surface of the baseplate and set the stencil on the baseplate as shown in Figure 4.1(a).

Step2：Apply the grease

Apply the grease to the edge of the stencil as shown in Figure 4.1(b), ensuring it spreads evenly across the entire surface of the baseplate.

Step3：Squeeze the Grease

As shown in Figure 4.1(c), use a squeegee to press the grease into the stencil. Figure 4.1(d) shows the state of the grease after squeezing.

Step4：Remove the Stencil

After squeezing, as shown in Figure 4.1(d), remove the stencil.

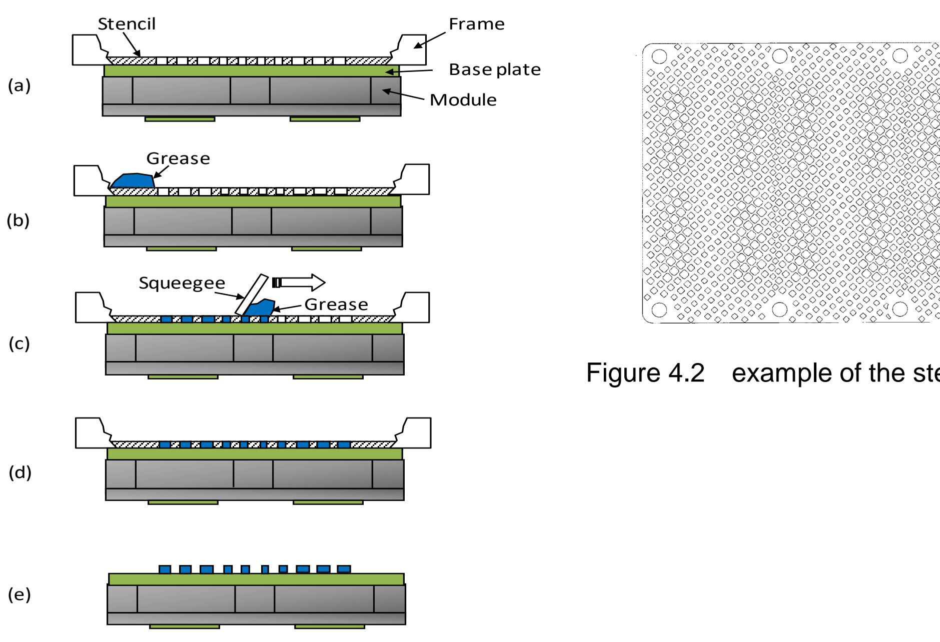


Figure 4.2 example of the stencil pattern

Figure 4.1 workflow of coating thermal grease

4-1-3. **Recommended Screw Tightening Sequence**

For preliminary and final tightening of modules with 4-point, 6-point, and 8-point screws, please follow the sequence shown in Figure 4.3.

Preliminary Tightening: Follow the sequence 1 ⇒ 2 ⇒ 3 ⇒ 4...

Final Tightening: Follow the sequence ...4 ⇒ 3 ⇒ 2 ⇒ 1

Note that the tightening sequence should follow a diagonal pattern, and there are no specific restrictions on the starting position. (The same applies for retightening.)

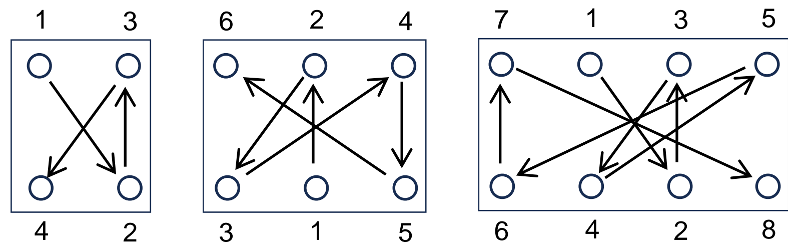


Figure4.3 Screw tightening sequence of IGBT modules.

If the tightening sequence and torque values shown in Figure 4.3 are not followed, the viscosity of the grease may cause the base to warp, which can lead to insulation breakdown of the insulating substrate inside the device.

Additionally, if the interval between temporary tightening and final tightening is too short, the viscosity of the grease may cause the base to warp, potentially resulting in insulation breakdown. Therefore, please ensure that the interval (waiting time) is properly observed. After installing the module, please confirm by performing an insulation withstand voltage test.

4-1-4.　Surface Roughness and Warping of the Heatsink, etc.

Important Notices

•The surface roughness of the heat sink, should be "25S" or higher.

•The convex or concave warp of the heat sink should not be more than 50μm (between the mounting screw holes).

• Confirm that the surface of the heat sink is free of burrs and be sure to chamfer the screw holes.

•Always be certain to look for and remove all foreign substances, such as cuttings, which may get caught between the IGBT module and heat sink.

4-1-5.　Mounting Holes for the Heatsink

If the diameter of the mounting holes in the heatsink is too large, the metal base of the IGBT module may deform, as shown in Figure 4.4, potentially damaging the chips inside the module. Therefore, please select an appropriate mounting hole diameter that matches the size of the screws being used. Table 4.2 shows the recommended mounting hole diameters and chamfer values for the screws.

Table 4.2　Recommended mounting hole diameter and chamfer value（mm)

№	Screw	Mounting hole diameter	Recommended chamfer value
1	M4	φ5	C0.5
2	M5	φ6	
3	M6	φ7.5	
4	M7	φ9.5	

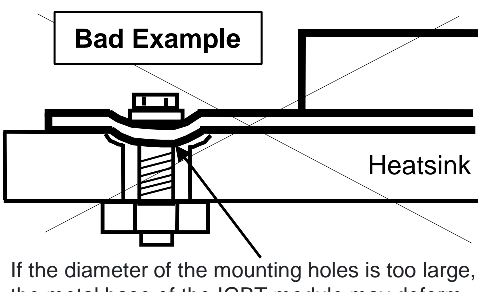


Figure 4.4　Example of mounting on an inappropriate heatsink

4-2.　Screw Mounting to the Terminals

4-2-1.　Handling of Terminals

Do not apply compressive or tensile stress of 147N (15kgf) or more per terminal to the main terminals. Additionally, for the main terminals of the nHPD^2 package, do not apply tensile loads of 50N per terminal or more in the tensile direction, and compressive loads of 250N per terminal or more in the compressive direction. Deformation of the module and main terminals may cause package damage or internal wiring short circuits.

Do not bend or flex the main terminals/auxiliary terminals. There is a risk of terminal breakage. Furthermore, if the structure is such that the terminals are used to support heavy objects, there is a risk of terminal breakage due to the applied load. Therefore, please conduct vibration tests on the actual equipment in advance to evaluate the structure.

4-2-2. Recommended Screw Tightening Sequence

There are no specific regulations regarding the tightening sequence of screws on the terminals.

4-2-3. Screw Tightening

Use a manual or electric screwdriver to tighten the screws with the recommended torque shown in Table 4.3.

Table 4.3 Torque for mounting screw terminals.

№	Screw	Rated torque (N・m)	Recommended torque (N・m)	Minimum torque (N・m)	Remarks
1	M4	2.0	1.8	1.6	Auxiliary terminal
2	M8	15.0	15.0	12.0	

4-2-4. **Recommended Screw Depth**

The cross-sectional view of the screw-type mounting section is shown in Figure 4.5. The recommended depth (length) of the screw should be selected so that the length "d" (protruding length from the nut) in the figure is 1-2mm.

The dimensions (a, b, c) in Figure 4.5 vary depending on the type of screw, as shown in Table 4.4. Note that these dimensions do not include the thickness of wiring or other materials.

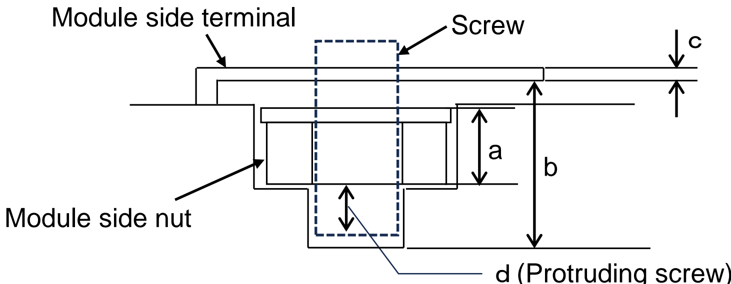


Figure4.5 Cross-sectional view of the screw hole on the module side.

Table 4.4 Length of each part of the screw hole in Figure4.5 (a, b, c)

No.	Screw	a(mm)	b(mm)	c(mm)	Remarks
1	M4	3.2	10.0	0.6	Auxiliary terminal
2	M8	8.0	17.0	1.5	

4-3. Design Reference for Busbar and Capacitor Connection

When attaching a capacitor to the DC terminals of a power module by a busbar, it is important to ensure that the stray inductance of the busbar is minimized. Large stray inductance may lead to a significant voltage spike during turn-on and off, which may exceed the V_{CES} rated voltage of the power module. When using the power module, care must be taken to ensure that the voltage, including the spike voltage, does not exceed the V_{CES} rated voltage of the power module. Additionally, the switching losses of the power module can vary depending on the structure of the busbar, leading to differences from the values listed in the specification sheet. Therefore, it is necessary to measure the electric characteristics under the real connection conditions of the inverter.

Figure 4.6 shows an example of connecting a busbar and capacitor to an nHPD^2 package. In this example, the DC busbar is designed with a laminated structure to reduce the stray inductance of the busbar. We uses a similar busbar design when evaluating the characteristics of power modules.

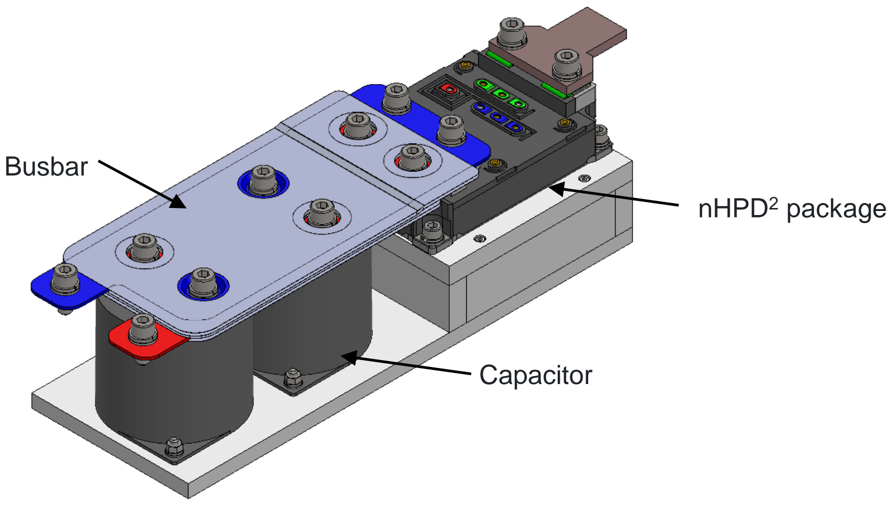


Figure 4.6 An example of connecting a busbar and capacitor to an nHPD^2 package

4-4. Busbar Mounting Precautions

Do not lift, bend, or pull the main or auxiliary terminals as they damage them. Additionally, in configurations where the terminals are used to support heavy loads, excessive load may damage the terminals. Be sure to evaluate the actual equipment by vibration test in advance..

When connecting multiple main terminals to the same busbar, perform preliminary tightening with approximately 30% of the recommended torque shown in Table 4.3 for all main terminals before performing the final tightening. When removing, ensure that each main terminal retains a torque approximately equal to the preliminary tightening torque until all main terminal bolts are loosened. Applying excessive torque to a specific main terminal without preliminary tightening may damage the case.

Figure 4.7 shows an example of busbar connection. When attaching or removing the busbar to/from the main terminals, fix the busbar at a part other than the main terminals to ensure that the tightening or loosening torque is not directly transmitted to the case. Excessive tightening or loosening torque applied to the case may cause it to break. When fixing the busbar to a support post or similar structure, ensure that the height is equal to or less than the height of the module. During connection, it is recommended that compressive load, rather than tensile load, is applied from the busbar to the module.

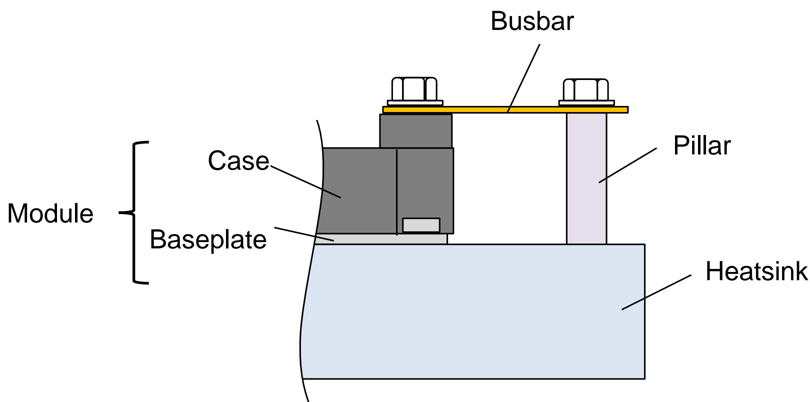


Figure4.7 Example of busbar mounting method to terminals

During operation of the power module, the module main terminals generate heat due to resistance. Part of this heat is dissipated through the bus bars. As a result, the temperature at the busbar connection part of the main terminals rises. When designing an inverter, it is necessary to consider the impact of temperature fluctuations and heat dissipation at the busbar mounting part of the main terminals on the reliability of the busbar and surrounding components. Figure 4.8 shows the relationship between the amount of heat dissipation from the main terminals and the temperature difference across the main terminals. Here, the amount of heat dissipation from the terminals is shown when a sinusoidal current of 1600A(peak) and 800A(peak) is passed through the AC terminals.

Additionally, the maximum temperature of the main terminals may occur inside the module depending on the operating conditions. Therefore, when large current is conducted, an upper limit may be set for the temperature at the busbar mounting part of the main terminals and the case temperature.

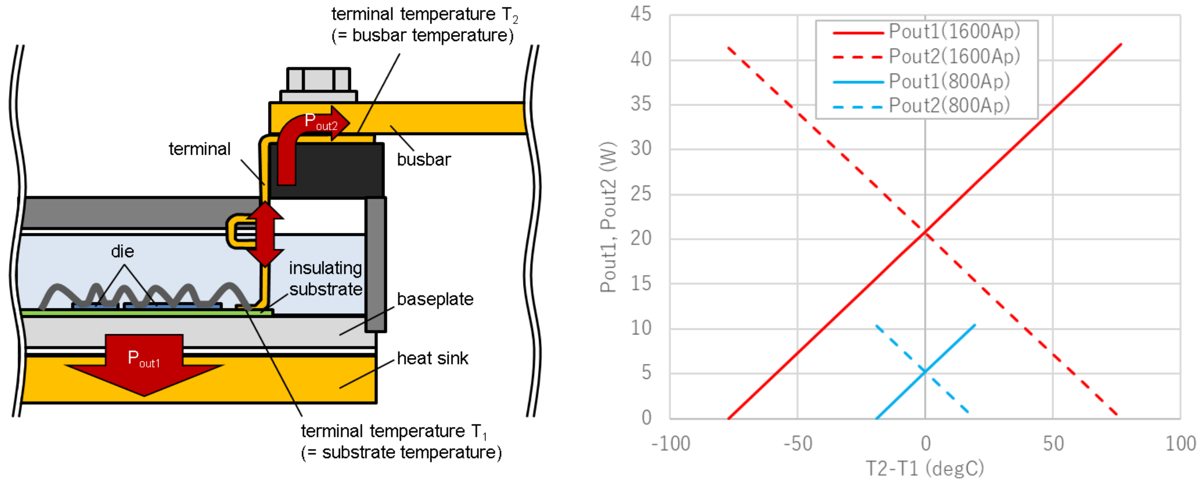


Figure4.8 Example of the relationship between heat dissipation from terminals and temperature difference across the terminals.

4-5. PCB Mounting

Table 4.5 shows the recommended tightening torque for the screw terminals when mounting a PCB on the top surface of the module, and Figure 4.9 shows the tightening sequence for the PCB mountings crews. After tightening the four corners A to D in the illustrated order, tighten the inner connection points 4 to 11 in any order. Regarding the screw length, refer to the screw hole depth dimensions provided in the outline drawing in the specifications, and adjust the length considering the thickness of the PCB to be used.

Additionally, for the PCB material, FR-4 (glass epoxy) substrate is recommended.

Table4.5 Recommended tightening torque for screw terminals of PCB mounting.

№	Screw	Rated torque (N・m)	Recommended torque (N・m)
1	M3	0.8	0.65±0.15

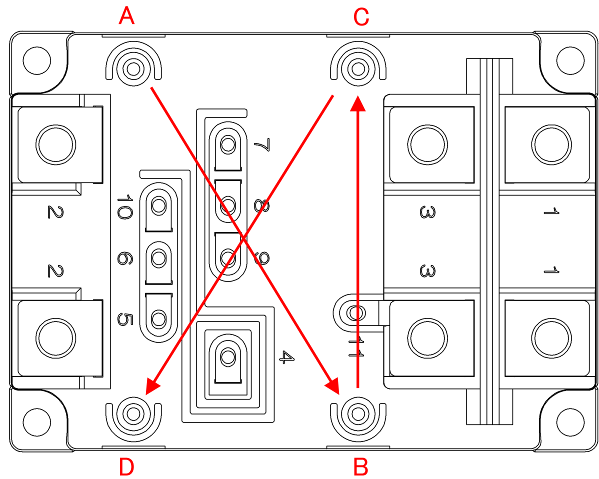


Figure4.9 Tightening sequence for PCB mounting screws.

4-6. Mounting Environment

Important Notices

Concerning the mounting environment for the module please be aware of the following.

●Harmful Substances：When an IGBT module is exposed to corrosive gases, such as sulfur dioxide or chlorine gas, conductivity or heat radiation may decrease because of terminal or base corrosion and parts may discolor. Make sure to always keep IGBT modules away from such substances.

●Exposure to Elements：Protect the IGBT module from both rain and water.

4-7. Storage and Shipping Precautions

Important Notices

(1) IGBT modules should always be stored under the following conditions.

●Temperature：40 degrees Celsius, maximum.

●Humidity：60％ Relative Humidity, maximum.

●Dust：Avoid storing the module in locations subject to dust.

●Harmful substances：The installation location should be free of corrosive gases such as sulfur dioxide and chlorine gas.

●Other：Do not remove the conductive sponges or tapes attached to the signal gate and emitter gate.

(2) Shipping Method

●To prevent the case cracking and/or the electrode bending, appropriate consideration should be given to properly insulate the shipping container from mechanical shock or sever vibration situation.

●Do not throw or drop the case while shipping. Treat them with care. The devices may break if they are not handled with care. Please do not use the IGBT modules that were dropped or damaged.

●Appropriate labeling on the outside of the shipping container should always be present.

●The shipping container itself should always be properly protected from both rain and water.

4-8. Precautions against Electrostatic Failure

Important Notices

Since IGBTs have a MOS gate structure, please pay close attention to the following points as electrostatic discharge (ESD) precautions:

- Do not remove the conductive metal or tape attached between the gate and emitter until the device is ready for use.
- When handling the device, ensure that the human body is grounded through a high resistance (approximately 100kΩ to 1MΩ), hold the package body, and avoid touching the gate terminals.
- Ensure that the workbench, soldering iron, and any other objects that may come into contact with the device are properly grounded.
- During testing and inspection, confirm that any residual charge in the measuring instruments has been removed. Additionally, when applying voltage to each terminal, start from 0V and return to 0V to finish.

4-9. Circuit Layout and Wiring Method for IGBT Modules

(1)IGBT Module Placement:

Place the IGBT module so as to minimize the wiring inductance from the power supply. If this wiring inductance becomes large, it may generate an overshoot voltage during switching and destroy the IGBT module. In order to reduce inductance of the main circuit wiring, please use laminated bus bars.

(2)Gate Circuit Wiring:

keep the cable between the gate circuit and IGBT module as short as possible. If the cable is long, gate voltage will rise or fall more slowly and the switching time will become longer. In addition, the likelihood of noise generation will be increased. In order to reduce wiring inductance and prevent noise, either a two-wire stranded cable or shielded cable should be used.

4-10. Measurement Precautions

(1) V_{CES} Measurement:

Before beginning VCES measurements, be sure to short-circuit the signal gate and emitter terminals. If the signal gate and emitter terminals are kept open or their contact is defective during measurement, the IGBT module may be damaged. In addition, if there is a risk of condensation on the module due to a heat cycle test or other factors, after drying for more than 2 hours at approx. 100℃, measure within the specified temperature conditions.

(2) Voltage Differences During Switching:

Because IGBT modules have wiring between the chip inside the module and the module terminals, the voltage applied to the chip and the voltage of the external terminal is not identical, especially during switching.

For expressing the time rate of change in current as di/dt and the cable inductance as L, an inductive voltage equal to L × di/dt will be generated within the cable. Typically, cable inductance L is about 20 to 40 nH. So when the IGBT module is turned ON, the external terminal voltage observed is higher than the voltage applied to chip.

Conversely, when the IGBT module is turned OFF, the observed external terminal voltage is lower than the voltage applied to the chip.

5. Reliability

General matters and terminology are explained in this chapter.

In addition, reliability test items and content specific to the module structure are explained.

5-1. Failure Rate

In general, the failure rate of semiconductor devices changes with time as shown in Figure 5.1.

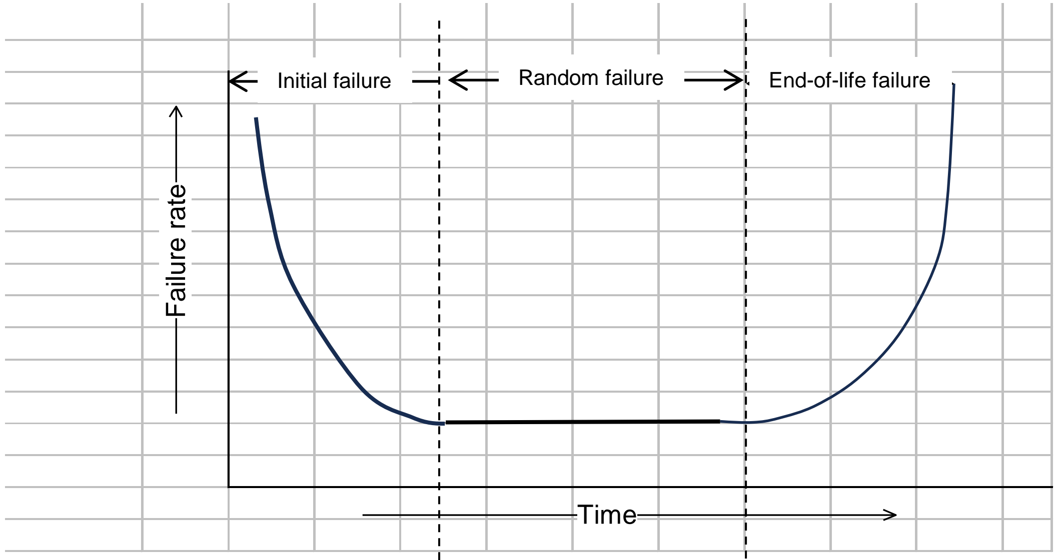


Figure 5.1Module Failure Regions (Bathtub-Shaped Curve)

Initial failure: failure that occurs at a relatively early stage due to design and production or incompatibility with the usage environment.

Random failure: failure that occurs incidentally after the initial failure period but before the end-of-life failure period.

End-of-life failure: failure that occurs during the period when the failure rate increases with time due to fatigue, wear, and degradation.

5-2. Failure Factors

Factors that determine the likelihood of the failure of semiconductor parts can be divided into external factors of use and internal factors of construction as shown in Table 5.1.

If failures such as those shown in the following table occur, analyze the factors that caused them and take appropriate countermeasures.

Table 5.1 Failure factors

Failure Factor		Examples
Internal Factors	Materials and Structures of parts	(1)Intermetallic compound generation failure （purple plague etc.） (2)Mismatching of thermal expansion rate
	Deviation in Product Process	(1)Failure of Al wire bonding （depends on position, pressure, crack etc.） (2)Scratch of die surface pattern (3) Failure of solder
External Factors	Thermal Stress	(1) Wear degradation and destruction due to thermal expansion (2) Facilitation of chemical change (compound generation, etc.)
	Electrical Stress	(1) Isolation breakdown (package) (2) ESD destruction of the IGBTs (For a die with a MOS structure)
	Mechanical Stress	(1) Connection bending (2) Package cracking (3) Isolation breakdown (package)
	Chemical Stress	Rust on external electrode
	Radiation	Change in device electrical characteristics due to accumulation of surface electric charge

5-3. Reliability Test

The types and contents of reliability tests conducted for our high-voltage IGBT module MBM450FS33F are shown in Table 5.2.

Table 5.2 The types and contents of reliability tests conducted for MBM450FS33F.

Test items	Test Conditions	Sample Size	Number of Failure	Judgment
High Temp. Storage	Temp. ; 150 deg.C Test Duration ; 1,000 hours	6	0	Pass
Low temp. Storage	Temp. ; -55 deg.C Test Duration ; 1,000 hours	6	0	Pass
Temp. Cycle	Temp. ; -40→25→125→25 all in deg.C Hold Time ; 60 minutes each condition Number of Repetition cycles ; 200	6	0	Pass
Temp. Humidity Storage	Temp. ; 60 deg.C Relative Humidity ; 90% Test Duration ; 1,000 hours	6	0	Pass
*Vibration(1) Variable Freq.	Acceleration ; 98m/s^2 Frequency Range ; 100-2,000Hz Sweeping Rate ; Approximately 20 minutes Sweeping method ; Logarithmic Test Time,Direction ; 2 hours of each X,Y,Z	6	0	Pass
*Vibration(2) Variable Freq.	Amplitude ; 1.5mm Frequency Range ; 10-55Hz Sweeping Rate ; Approximately 1 minutes Sweeping method ; Logarithmic Test Time,Direction ; 2 hours of each X,Y,Z	6	0	Pass
*Vibration(3) Fixed Freq.	Acceleration ; 98m/s^2 Frequency Range ; 60±20Hz Test Time,Direction ; 32 hours of each X,Y,Z	6	0	Pass
*Shock	Acceleration ; 980m/s^2 Pulse Width ; 6ms Test Time,Direction ; 3 cycles of each X,Y,Z	6	0	Pass
*Mounting Strength	Mounting Torque ; 6N・m Accessories ; aluminum heat sink(convex;100μm) Test Duration ; 336 hours	6	0	Pass
Terminal Strength	Torque of Screw Terminal ; 15N・m Accessories ; copper plate(5mmt) Test Duration ; 336 hours	6	0	Pass
Temp. Bias(AC)	Temp. ; 150 deg.C Apply Voltage ; 3,300Vp(C-E) Test Duration ; 1,000 hours	6	0	Pass
Temp. Bias(DC)	Temp. ; 150 deg.C Apply Voltage ; 2,600VDC(C-E) Test Duration ; 1,000 hours	6	0	Pass
*Temp. Bias(AC)	Temp. ; 150 deg.C Apply Voltage ; 20Vp(G-E) Test Duration ; 1,000 hours	6	0	Pass
*Thermal Fatigue Test (Intermitted Operating Test)	Current ; Ic/IF=450Ap Temp. ; Tc=30⇔100deg.C Sinusoidal Waveform ; 180 deg conduction(IGBT) 90 deg conduction(FWD)	6	0	Pass
Power Cycle	Current ; Ic=450A Temp. ; ⊿Tj=80 deg.C Tjmax=150 deg.C	6	0	Pass
*Electrostatic Discharge	Capacitor C ; 200pF Resistance R ; 0Ω Test Voltage ; 200V	6	0	Pass
Isolation	Applied Voltage ; 6,000Vrms×10minutes	6	0	Pass

*Tested by equivalent structure type

5-3-1. Reliability Test Acceptance Criteria

The criteria for determining device degradation in the above reliability tests are based on the following items and acceptance values.

Table 5.3 Criteria for MBM450FS33F determining device degradation in reliability tests.

Devices : IGBT Modules		Type : MBM450FS33F		
Ratings	Vces : 3,300V Ic(DC) : 450A Tj : -50 deg.C ～ 150 deg.C	Accept. Limit	1. Ices, Iges	＜2×Rated Value
			2. Vce(sat), VFM	＜1.2×Rated Value
			3. Vge(to)	＞0.8×Rated Value
			Vge(to)	＜1.2×Rated Value
			4. Others	＜Rated Value (Upper Limit)
				＞Rated Value (Lower Limit)

5-4. Quality Assurance System

Our quality assurance system is shown in Figure 5.2.

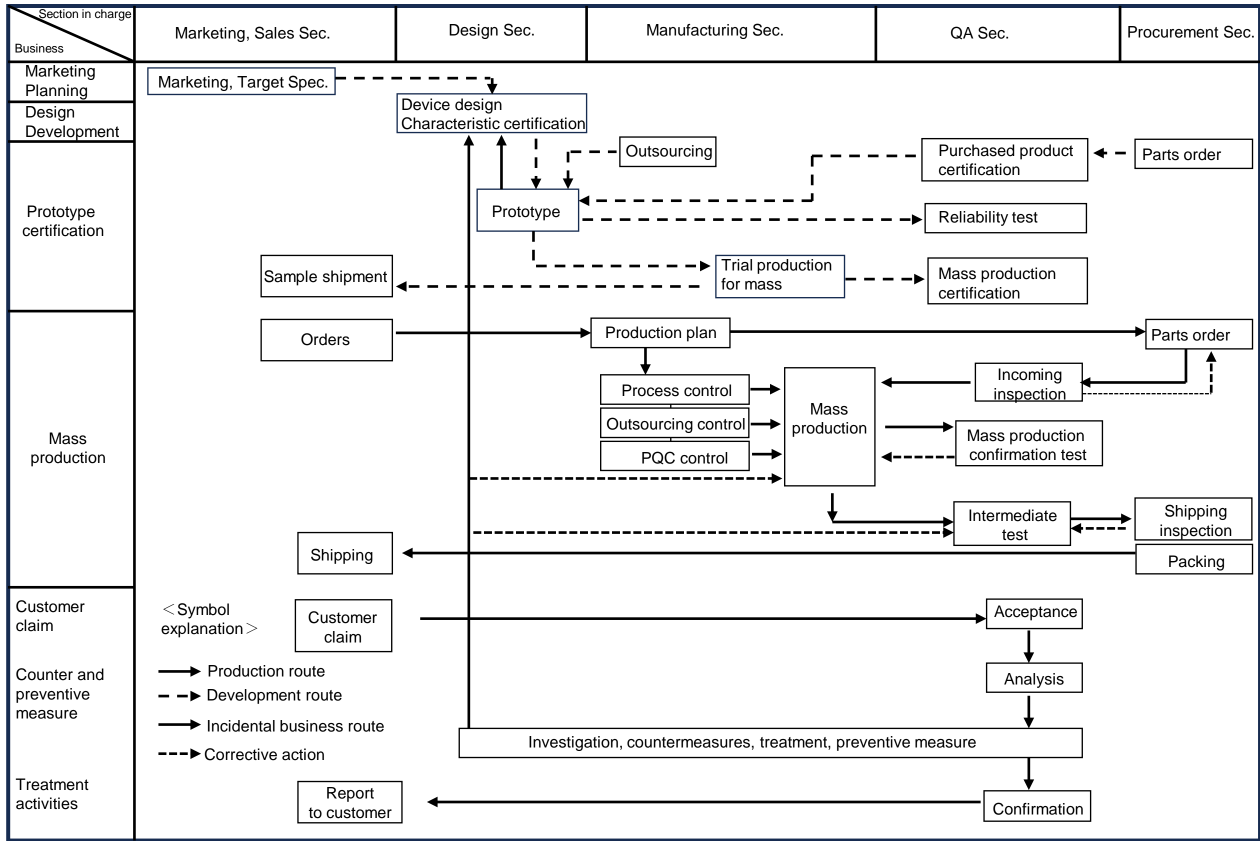


Figure5.2 Quality assurance system.

6. Troubleshooting

6-1. Failure Modes of IGBT Modules (Electrical Failure Modes)

When an IGBT fails, investigate the cause of the failure according to the following tree. However, please note that while this tree can assist in investigating the cause of IGBT failure, it does not necessarily guarantee that the cause can be identified.

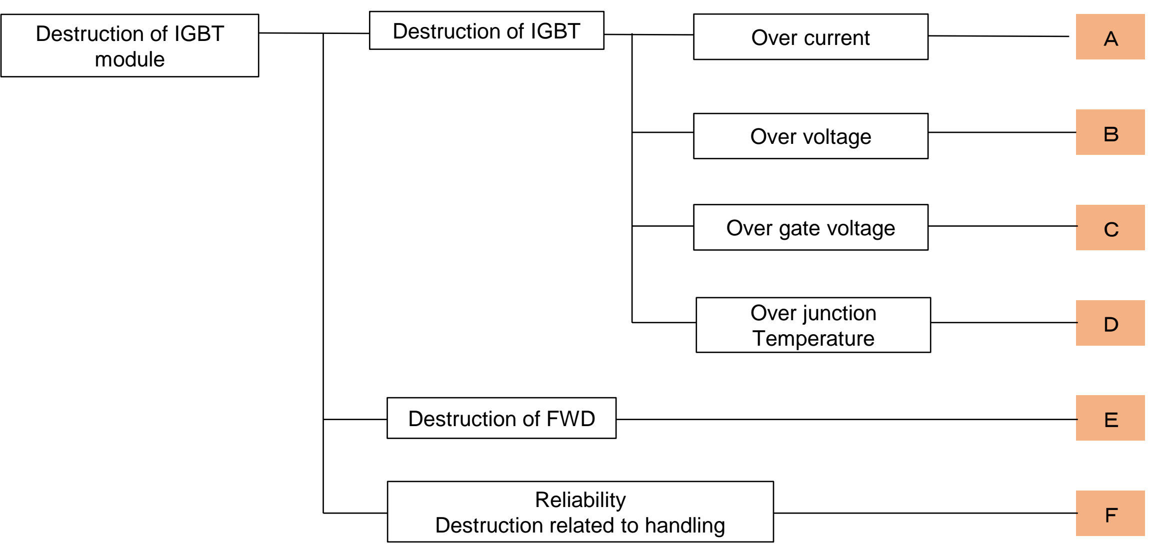


Figure 6.1 Failure modes of IGBT modules.

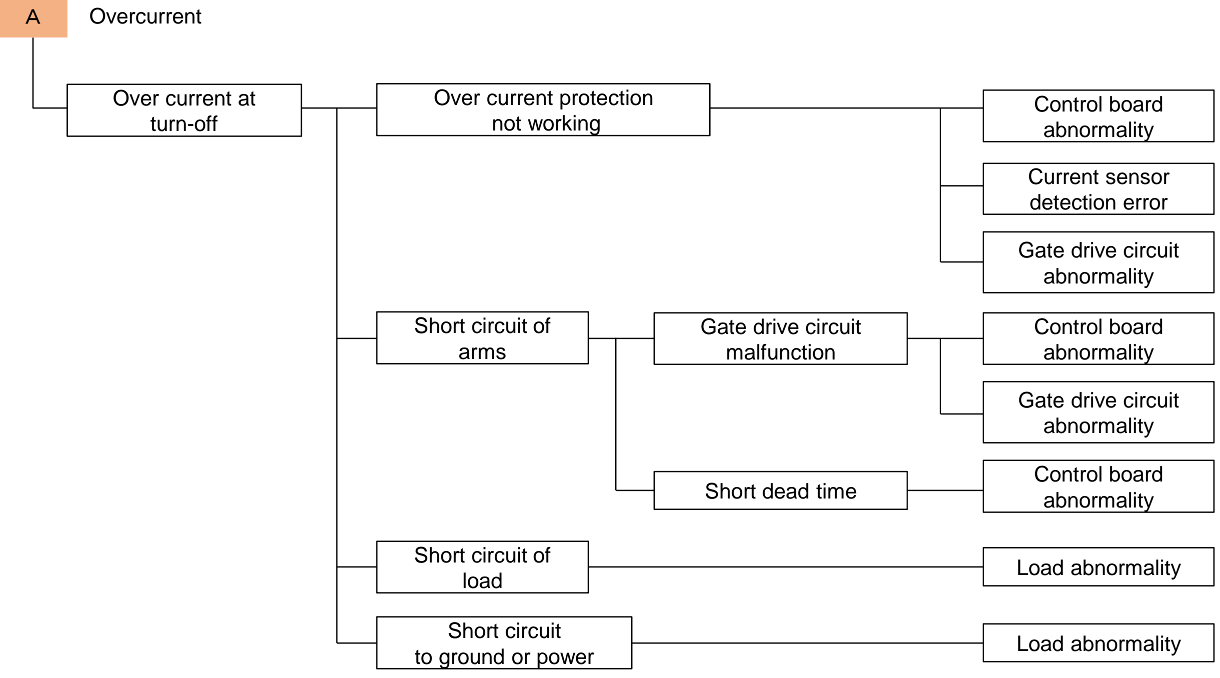


Figure 6.2 Failure Mode A:Overcurrent

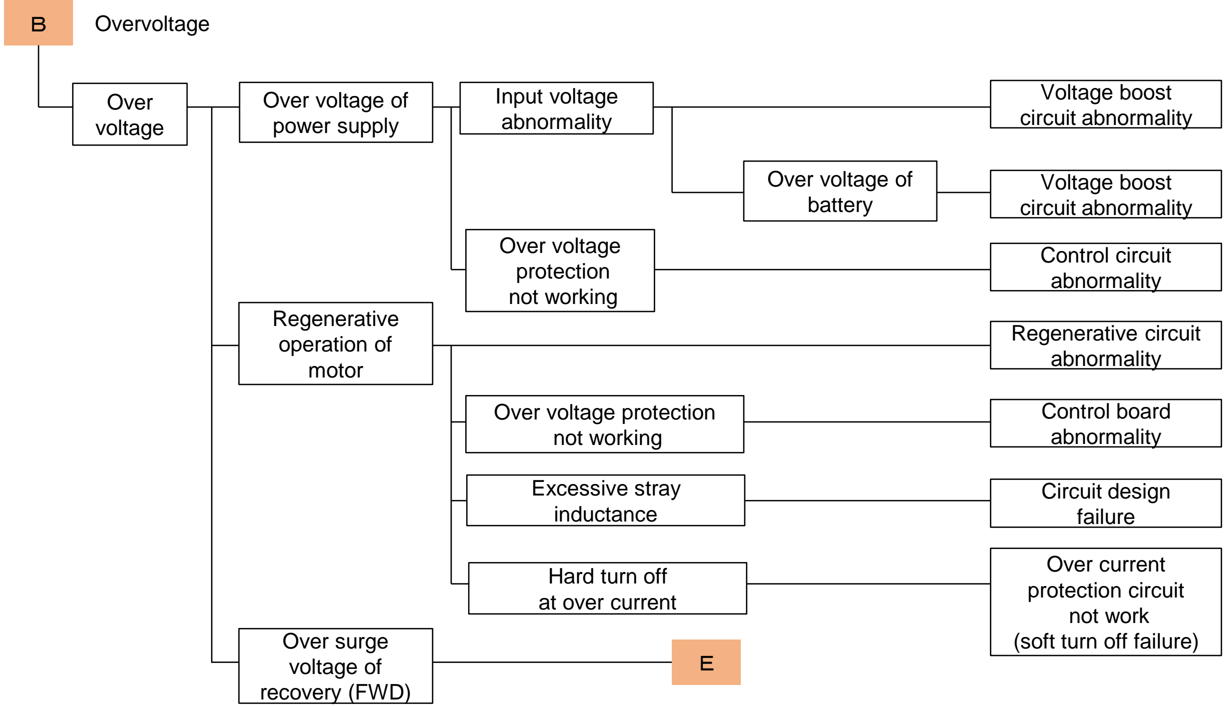


Figure 6.3 Failure Mode B: Overvoltage

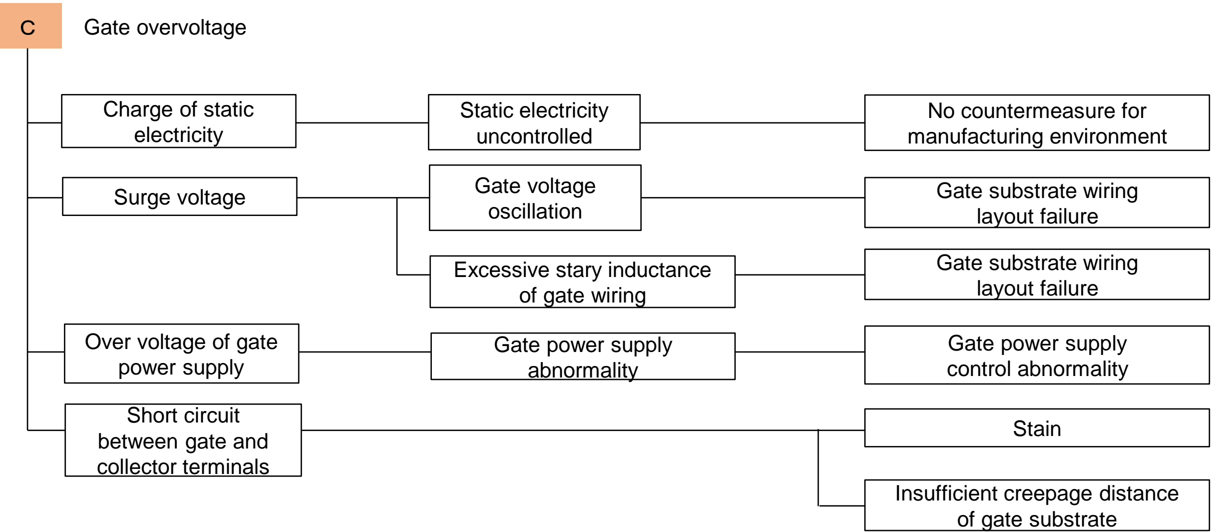


Figure 6.4 Failure Mode C:Gate overvoltage

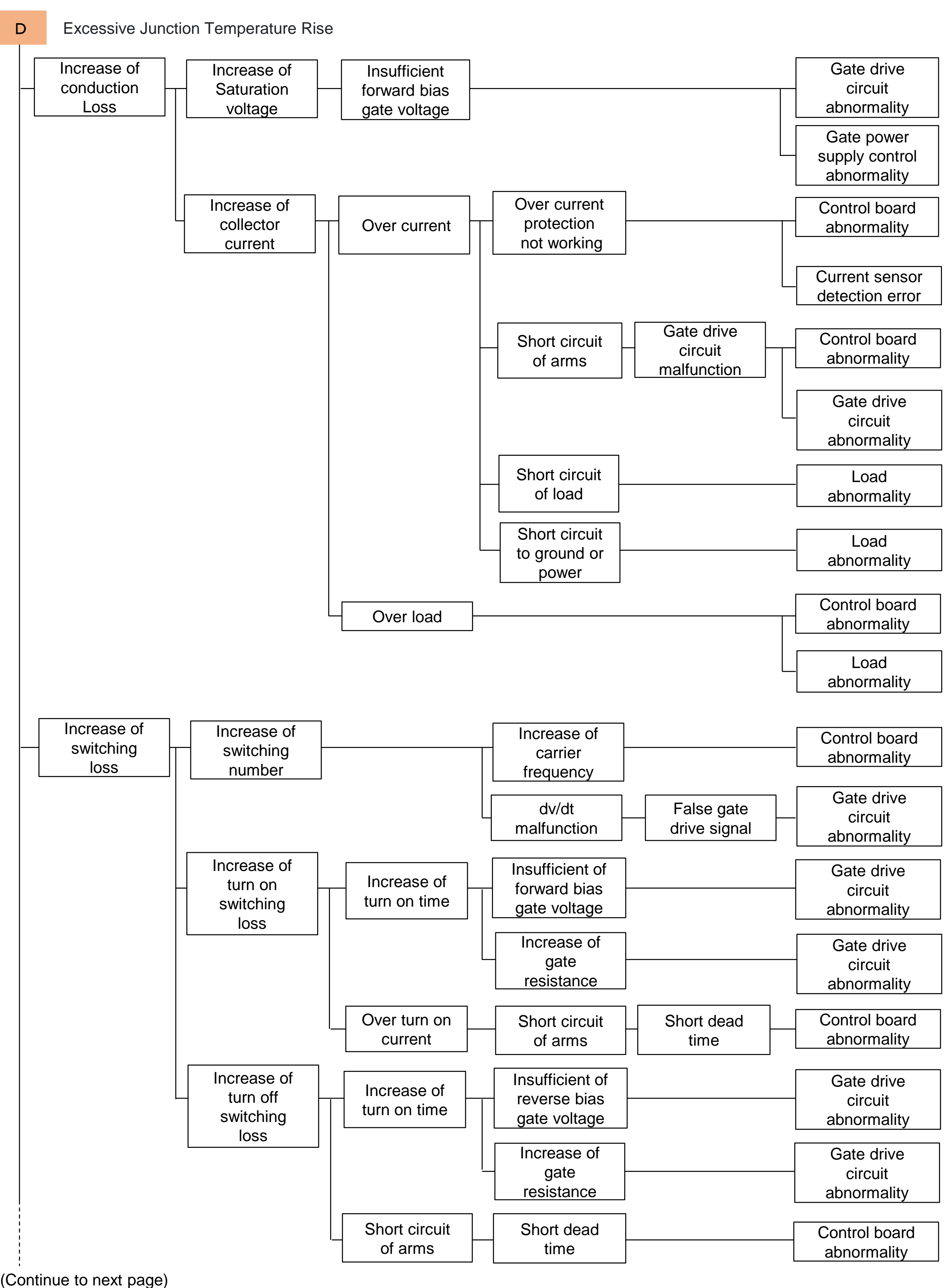


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Figure 6.5 Failure Mode D: Excessive Junction Temperature Rise (1)

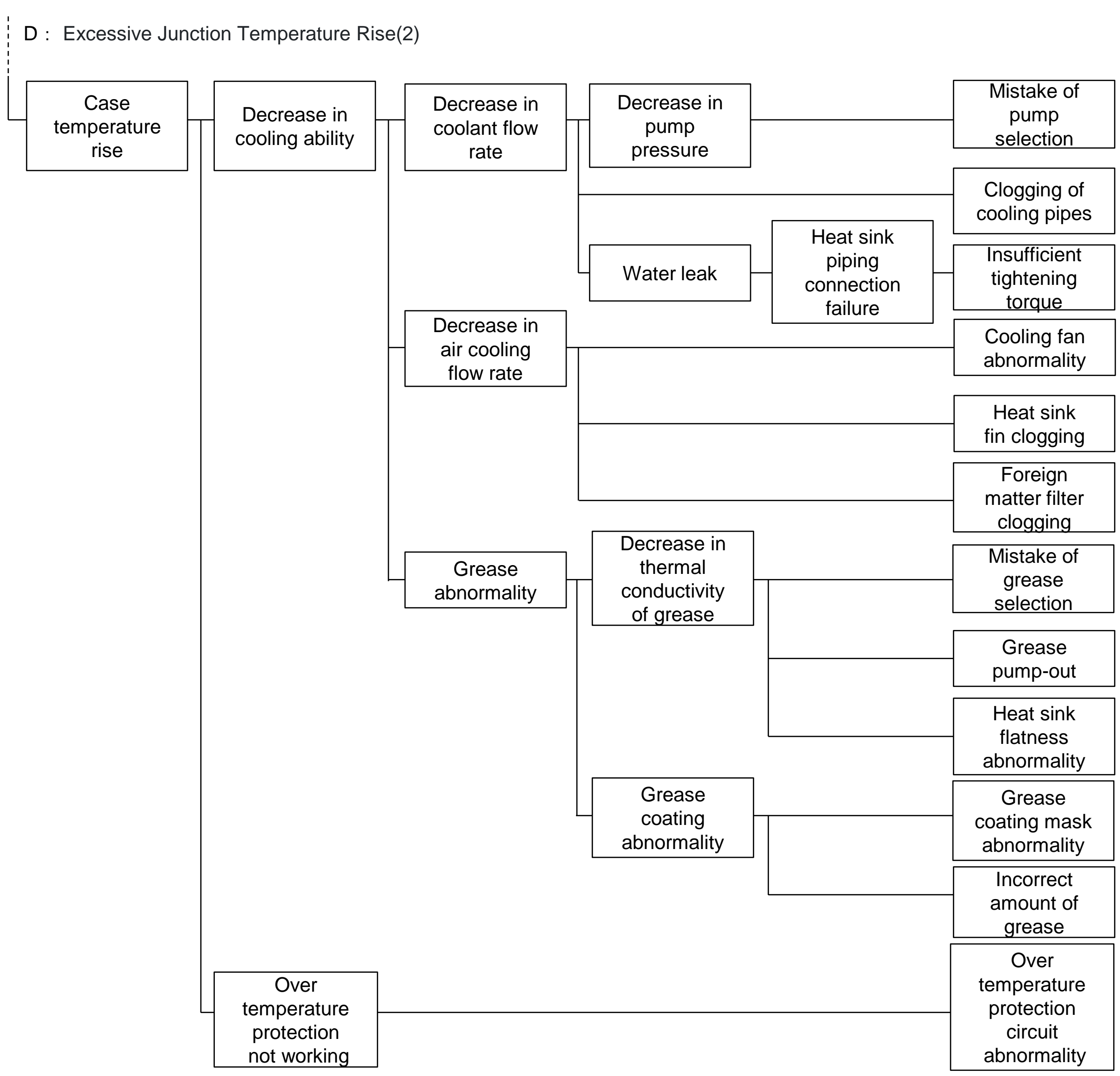

Figure 6.5 Failure Mode D: Excessive Junction Temperature Rise (2)

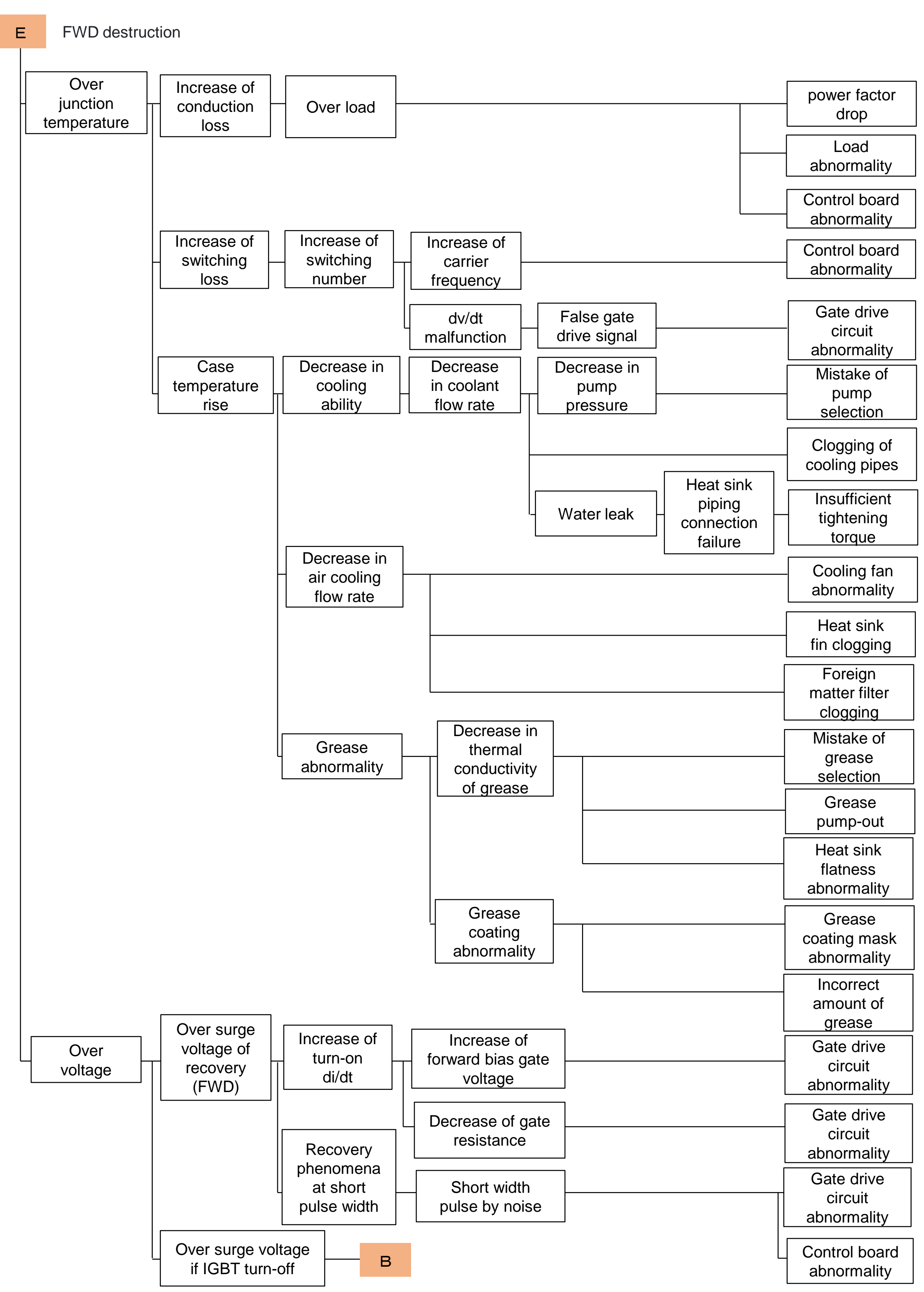

Figure 6.6 Failure Mode E: FWD destruction

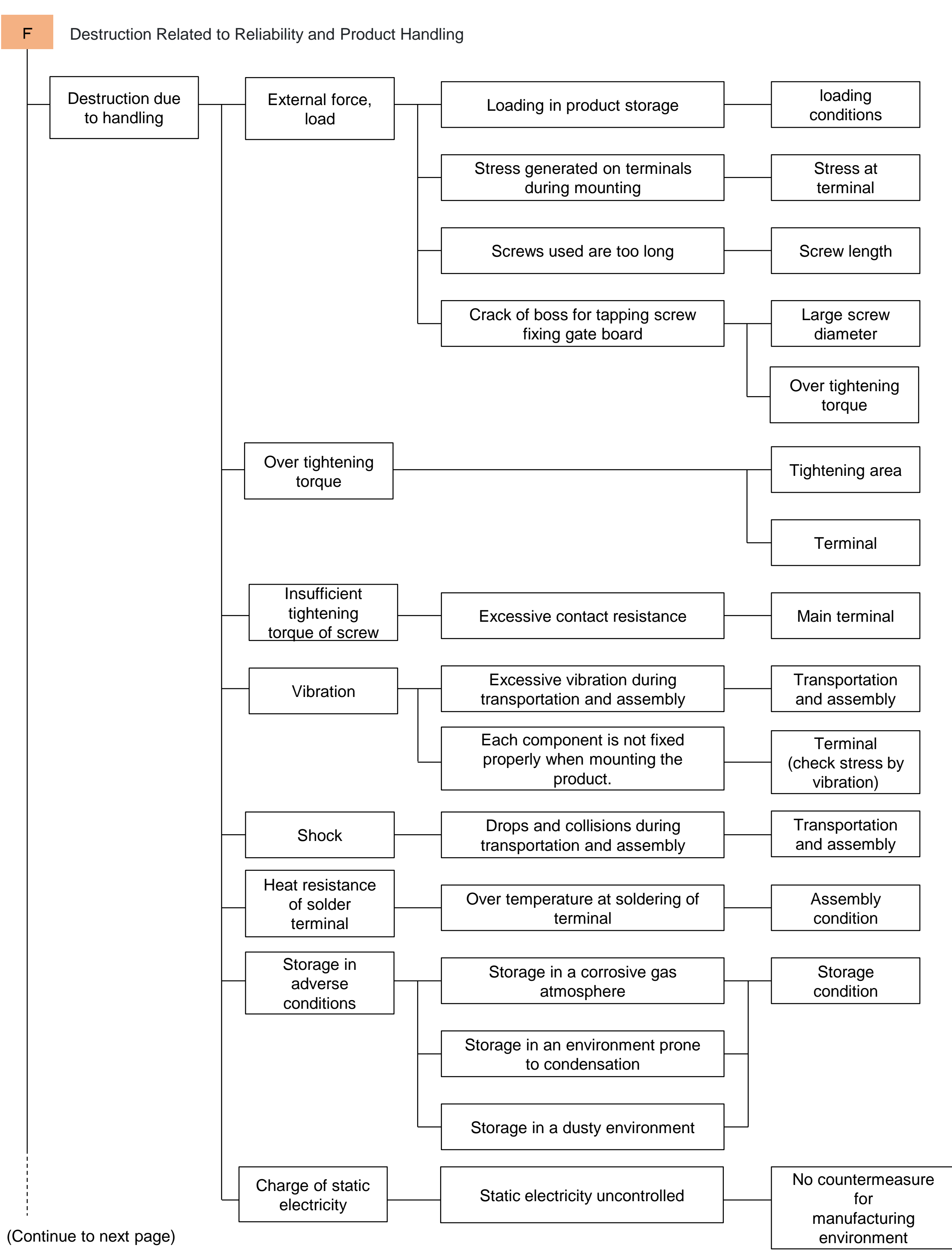

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Figure 6.7 Failure Mode F: Destruction Related to Reliability and Product Handling (1)

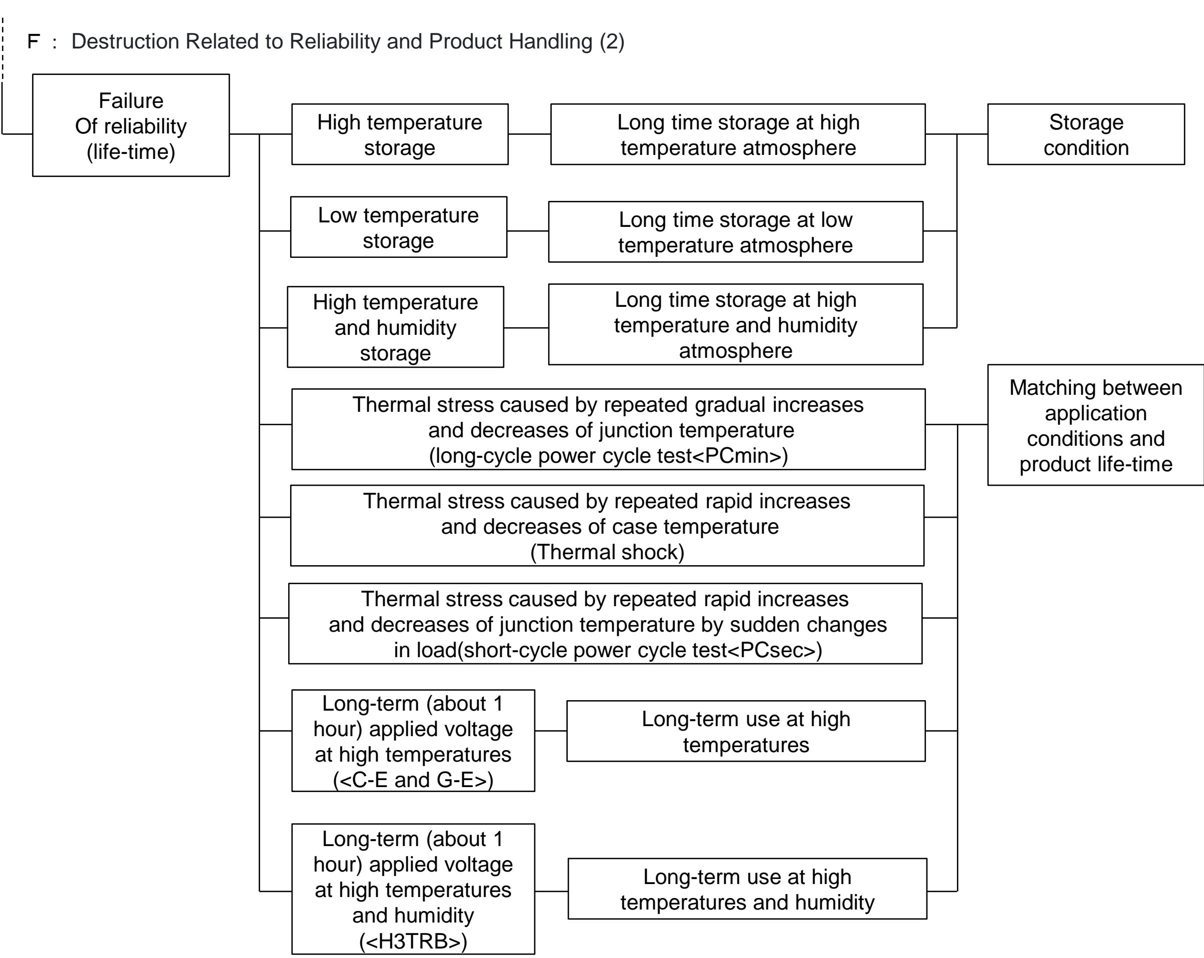

Figure 6.7 Failure Mode F: Destruction Related to Reliability and Product Handling (2)

6-2. Device Check

To check IGBT electrical characteristic, a “Curve Tracer” is generally used to measure voltage and current. Figure 6.1 shows both good and bad sample examples for checking IGBT module characteristics. In addition, please note that if the device has degraded or has been damaged, using this method may lead to secondary damage.

Table 6.1 Verifying Device Characteristics Methods

Table 6.1 IGBT Electrical Characteristic Check Method (Reference)

Checking terminal	Output waveform of Curve Tracer	
	good sample	failed sample
C to E (Requires G to E connection) C, G, E, E, +, −, Curve Tracer	ICE (～0.1mA/d) IGBT Breakdown voltage avalanche voltage leakage current 0 VCE (～200V/d) FWD forward voltage 《conditions of no failure》 leakage current ≦ spec. value avalanche voltage ≧ spec. value FWD Vb = 0.3V ICE, VCE, 0 Enlarge (1mA/d、0.5V/d) ICE ≦ 1 mA@ V=-0.3V (FWD built in voltage Vb)	ICE(1mA to several tens of mA/d) failure sample no failure sample resistive characteristics (several Ohms～) In case of IGBT short (resistive destruction)
G to E +, −, C, G, E, E, Curve Tracer	IGE (10 μA～ 1 mA/d) Current changing at VGE(TO) IGE = 0 at VGE max 0 VGE (1 V/d) displacement current depend on input capacitance In the case of no failure sample (An AC measurement mode of Curve Tracer is used.) 《Conditions of no failure》 Current changing at VGE(TO) IGE=0 at VGE max. no leakage current <max. value of spec to flow the displacement current depend on input capacitance	IGE (1 mA/d) no failure sample O (1 V/d) VGE characteristics failure of resistive mode In case of G to E short, breakdown voltage failure of C to G
C, G to E (This is a test to verify that the IGBT is turned on.) +, −, C, G, E, E, Curve Tracer	I (10mA～/d) IGBT Forward voltage to appear the FWD forward characteristics 0 V (1～2V/d) begin to flow the IGBT current at V ≒ VGE(TO) current ≒ 0 FWD Forward voltage 《conditions of no failure》 Begin to flow the IGBT current at VGE =VGE(TO) to appear the FWD forward characteristics (built in voltage)	I (10mA～/d) O V (1～2V/d) no failure sample begin to flow the IGBT current at V < VGE(TO) in case of failure sample In case of VGE(TO) failure

*1. In this case, we described the measurement mode of the curve tracer as AC (alternating current power output), but if necessary, observe as DC mode (positive or negative voltage output).

You may wish to use DC mode to make it easier to observe leakage failure due to the low displacement current.

*2. Verifying characteristic failure of the module due to isolation voltage or temperature change is difficult using this method.

*3. Module characteristics checks with testers with low power supply voltage (simple testers with a few Vs) is also possible, but in such cases, it is difficult to "fully understand" the condition of the module.

7. Failure Precautions

7-1. **Warnings**

7-1-1. Precautions for Package Bursting

Warning

●When either a load- or arm- short circuit occurs in an IGBT module, it must be turned OFF immediately (within a few microseconds). Otherwise, the module case may burst.

This is because energy at the time of short circuit accumulates in the module and will be released instantaneously.

Always be certain that you take the following precautions:

1) Keep the IGBT module in a closed case to prevent operator harm should it ever burst.
2) Never open the IGBT module's closed case while an electric current is being supplied to the module.

7-1-2. Warnings Regarding Burns and Electric Shock

●Do not touch or approach the product while when it is powered on. There is a risk of burns and electric shock.

7-2. Caution

Caution

● After the IGBT breaks down, ensure that a short-circuit current does not continue flow for a long time (several hundred microseconds). There is a risk of smoke and ignition.

Although the resin of the IGBT module uses UL94V-0 flame-retardant class material, please protect it with a fuse.